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Design of Fault Tolearnt Reversible Full Adder/Subtarctor

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Abstract: Reversible logic is emerging as an important research area having its application in diverse fields such as low power CMOS design. The paper proposes the design of full Adder/Subtractor circuit using fault tolerant reversible logic gates. The design can work singly as a reversible Full Adder/Subtractor unit. It is a parity preserving reversible adder cell, that is, the parity of the inputs matches the parity of the outputs. The proposed parity preserving reversible adder can be used to synthesize any arbitrary Boolean function. It allows any fault that affects no more than a single signal readily detectable at the circuit's primary outputs. The proposed design offers less hardware complexity and is efficient in terms of gate count, garbage outputs and constant inputs than the existing counterparts.

Keywords: Reversible gate, Feyman double gate, Fredkin gate, full adder, delay

I. INTRODUCTION

The decimal arithmetic is receiving significant attention as the financial, commercial, and internet-based applications cannot tolerate errors generated by conversion between decimal and binary formats [1]. Since the decimal arithmetic is getting significant attention, specifications for it have recently been added to the draft revision of the IEEE 754 standard for floating-point arithmetic; IEEE 754r is an ongoing revision to the IEEE 754 floating point standard [2, 3]. The major consideration while implementing adder circuit will be to enhance its speed as much as possible. Researchers like Landauer have shown that for irreversible logic computations, each bit of information lost, generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [4]. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [5], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation.

Reversible circuits are those circuits that do not lose information and reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors. The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are also of high interest in optical computing, nanotechnology and quantum computing. The most prominent application of reversible logic lies in quantum computers. In quantum computer, any unitary operation is reversible and hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND & OR are clearly irreversible). One of the major constraints in reversible logic is to minimize the number of reversible gates used and garbage outputs produced (Garbage output refers to the output that is not used for further computations). Synthesis of reversible logic circuits differs from the combinational one in many ways [6]. Firstly, in reversible circuit there should be no fan-out, that is, each output will be used only once. Secondly, for each input pattern there should be a unique output pattern. Finally, the resulting circuit must be acyclic. Any reversible gate performs the permutation of its input patterns only and realizes the functions that are reversible. If a reversible gate has *k* inputs, and therefore *k* outputs, then it is a *k***k* reversible gate. Any reversible circuit design includes only the gates that are reversible. An efficient design should keep the number of garbage outputs to minimum. Parity checking is one of the widely used error detection mechanisms in digital logic and data communication systems.

This is because most of the arithmetic functions is not parity preserving. If the parity of the input data is maintained throughout the computation, no intermediate checking would be required [7]. A sufficient requirement for parity preservation of a reversible circuit is that each gate be parity preserving [7].

Thus, we need parity preserving reversible logic gates to construct parity preserving reversible circuits. This paper

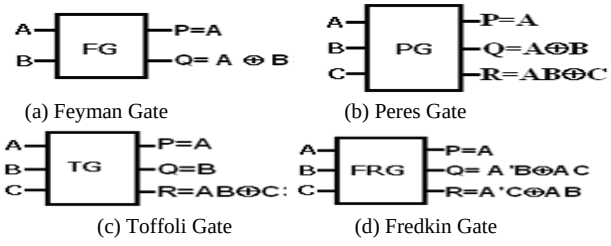
presents a new full adder/subtarctor design having parity preserving logic through use of reversible parity preserving reversible logic gates. It is parity preserving, that is, the parity of the inputs matches the parity of the outputs. The presented design does not produce any unnecessary garbage outputs. Minimizing number garbage outputs are the major concern in reversible logic design [6]. The presented fault tolerant full adder block can be used to realize other arithmetic circuit such as ripple carry adder, carry look-ahead adder, carry-skip logic, and multiplier/divisors.

The paper is organized as follows: the section II covers the short review on reversible gate concepts and its types. Section III covers the proposed design of adder/subtarctor. Section IV is the results and discussion part followed up by conclusion in section V.

II. SHORT REVIEW ON REVERSIBLE GATES

A. Basic Reversible Gates:

There exist many reversible gates in the literature. Among them 2*2 Feynman gate (FG) [9], depicted in Fig. 1a, 3*3 Peres gate (PG) [10], depicted in Fig. 1b, 3*3 Toffoli gate (TG) [8], depicted in Fig. 1c and 3*3 Fredkin gate (FRG) [9], depicted in Fig. 1d have been studied extensively. Because of their simplicity and low cost there are design approaches and tools that incorporate them separately or in combination with each other [6], [8].



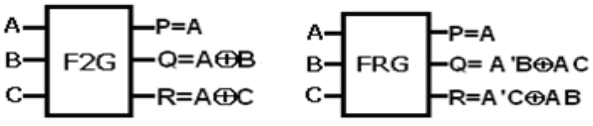
(a) Feyman Gate (b) Peres Gate

(c) Toffoli Gate (d) Fredkin Gate

Figure 1. Few preferred Reversible Gates

B. Parity Preserving Reversible Gates:

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of some its components. If the system itself made of fault tolerant components, then the detection and correction of faults become easier and simple. In communication and many other systems, fault tolerance is achieved by parity. Therefore, parity preserving reversible circuits will be the future design trends to the development of fault tolerant reversible systems in nanotechnology. And a gating network will be parity preserving if its individual gate is parity preserving [7].



(a) Feyman Double Gate (F2G) (b) Fredkin Gate (FRG)

Figure 2. Basic Parity preserving reversible Gates

A few parity preserving logic gates have been proposed in the literature. Among them 3*3 Feynman Double gate (F2G) [7] depicted in Fig. 2a and 3*3 Fredkin gate (FRG) [12] depicted in Figure 2b are one-through gates, which means one of the inputs is also output.

Table1. Table of Parity Preserving Feyman Double Gate (F2G)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Table2. Table of Parity Preserving Fredkin Gate (FRG)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

From Table 1 and 2, it can be seen that the gates F2G and FRG are parity preserving respectively; since they satisfy $A \oplus B \oplus C = P \oplus Q \oplus R$. And any k*k reversible logic gate where the EX-OR of the inputs matches the EX-OR of the outputs will be parity preserving.

III. PROPOSED WORK

Reversible logic implementation of adder circuit has been studied by several authors in the literature [6-7], [13]. It has been demonstrated in [6] that a reversible adder circuit can be realized with at least two garbage outputs and one constant input. This requirement is not the same for fault tolerant reversible various adder circuit. Because in a fault tolerant adder circuit the input parity must matches the parity of the outputs. This section first detail about the design of half adder/subtractor module using which other circuits will be designed keeping in mind to have minimum number of garbage outputs and constant inputs required. The paper proposes a new fault tolerant full adder/subtractor circuit followed by design of serial binary adder/subtractor circuit.

A. Design of Half Adder/Subtarctor circuit (FTHA_S):

For design of such unit the basic parity preserving reversible gates used is feyman double gate and fredkin gate as detailed in earlier section. The standard expression for Boolean expression for half adder is:

$$Sum = A \oplus B \quad (1)$$

$$Carry = AB \quad (2)$$

The Boolean expression for half subtarctor is:

$$Difference = A \oplus B \quad (3)$$

$$Borrow = \bar{A}B \quad (4)$$

From expression it can be observed that equation (1) & (3) are same. The only differences lie in carry & borrow expression. To implement a circuit which can act as both adder & subtractor under control of any control line has been

proposed in this section. The Fig. 3 details the proposed architecture which uses the feyman double gate and fredkin gate which is not only reversible but also has property of parity preserving. There are two inputs A and B and a control line ctrl which controls its mode of operation. When control signal ctrl is at logic 0, the circuit acts as half adder & when ctrl goes to logic 1, the circuit performs subtraction. The sum & difference line in shown as S/D and its carry & borrow signal is represented by C/B. The rest of four inputs which is said as constants is forced to logic 0 whereas the garbage signals are g1 to g5. From Fig. 4, it can be seen that the fault tolerant half adder/subtarctor (FTHA_S) circuit posses seven inputs and correspondingly seven outputs as per reversible rule. The proposed circuit can perform addition and subtraction with the use of only single circuit which is not advantageous in terms of power saving but also in terms cost. The Boolean expression of proposed circuit is:

$$S/D = A \oplus B \quad (5)$$

$$C/B = \overline{ctrl}AB + ctrl\,\overline{A}B \quad (6)$$

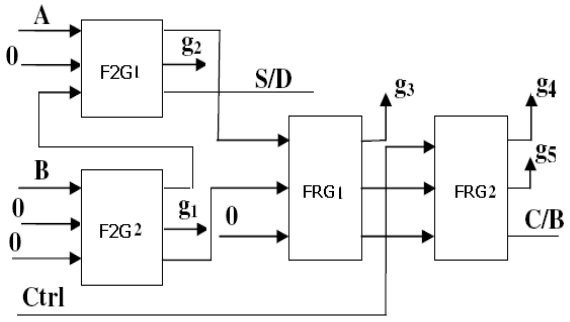


Figure 3. Circuit of reversible fault tolerant Half Adder/Subtractor

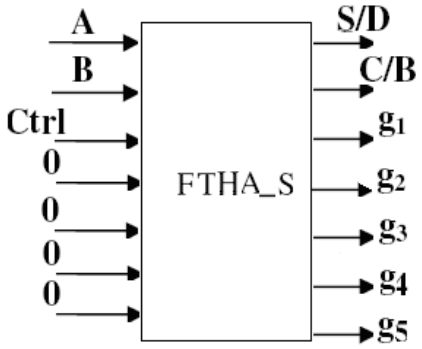


Figure 4. Half Adder/Subtarctor circuit with four constant inputs & five garbage outputs

B. Design of Full Adder/Subtarctor circuit (FTFA_S):

For design full adder/subtractor circuit the conventional approach is followed, that is using two half adder circuits. The full adder/subtractor using proposed FTHA_S circuit is shown in Fig. 4. The expression for full adder is:

$$Sum = A \oplus B \oplus C_{in} \quad (7)$$

$$Carry = A \oplus B\ C_{in} \oplus AB \quad (8)$$

The expression for full subtarctor is:

$$Difference = A \oplus B \oplus B_{in} \quad (9)$$

$$Borrow = \overline{A}B + BB_{in} + B_{in}\overline{A} \quad (10)$$

The equation (7) and (9) in same whereas there is difference in (8) and (10). The Fig. 5 details the proposed architecture which uses the proposed half adder/subtractor. There are three inputs A, B, Cin & a control line ctrl which controls its mode of operation. When control signal ctrl is at logic 0, the circuit acts as full adder & when ctrl goes to logic 1, the circuit performs subtraction. The sum & difference line in shown as S/D and its carry & borrow signal is represented by C/B. The rest of nine constant inputs are forced to logic 0 whereas there are eleven garbage signals. The proposed fault tolerant full adder/subtractor (FTFA) circuit can perform addition and subtraction with the use of only single ctrl.

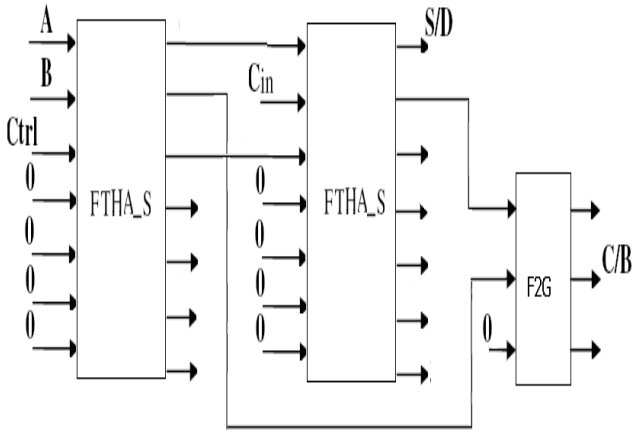


Figure 5. Circuit of reversible fault tolerant Full Adder/Subtractor

IV. RESULTS AND DISCUSSION

The entire architecture is modeled using VHSIC hardware description language (VHDL). The coding is done on Xilinx ISE8.2i on Spartan 3E using target device: 3s500efg320-4 at speed grade of -4. For simulation purpose the Modelsim6.2h has been used. The simulation result for FTHA and FTFA is shown on Fig. 6, Fig. 7and Fig. 8 respectively.

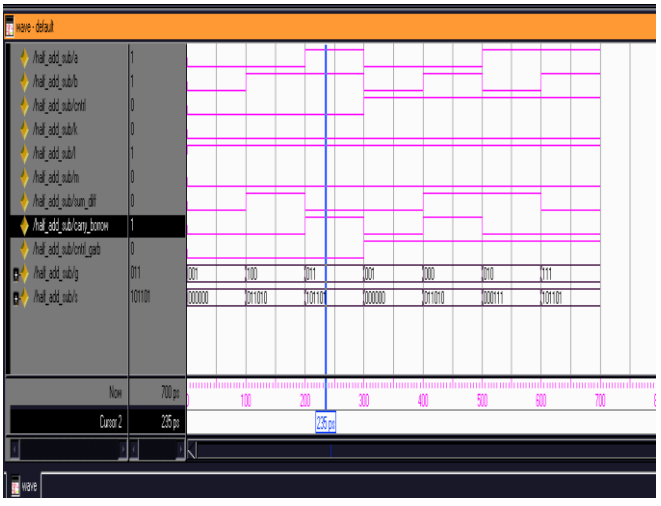


Figure 6. Simulation result of proposed half adder/subtarctor when cntrl=0 (acts half adder) & when cntrl=1 (acts half subtarctor)

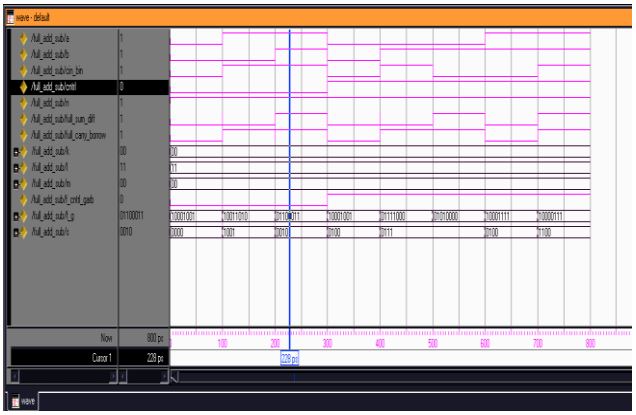


Figure 7. Simulation result of proposed Full Adder/Subtarctor circuit when cntrl=0 (acts as full adder)

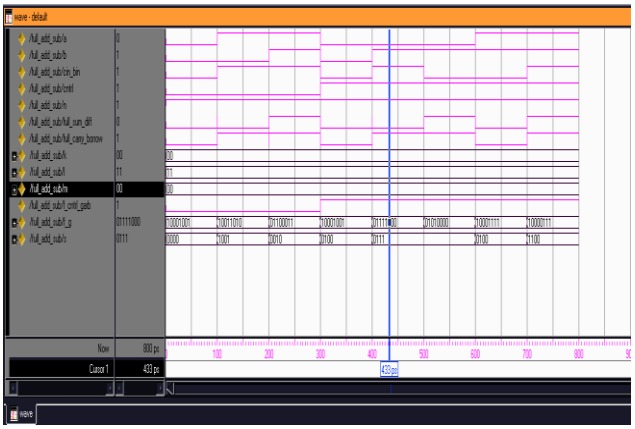


Figure 8. Simulation result of proposed Full Adder/Subtarctor circuit when cntrl=1 (acts as full subtarctor)

V. CONCLUSION

Computer hardware has grown in power at an amazing pace ever since. One of the most important computational resources is energy. The energy consumption in computation turns out to be deeply linked to the reversibility of the computation. A computation is called reversible if its inputs can always be deduced from its outputs. The primary objective of this paper was to gain insight into the Reversible Computation and its use for making devices energy efficient for long life. All computations can be done, in principle, for zero cost in energy.

The proposed circuit is design of single unit which can behave as adder as well as subtractor depending on requirement. Using such circuit can be helpful not in terms of power saving but also help in reducing cost.

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