Volume 2, No. 2, Mar-Apr 2011
ISSN No. 0976-5697
International Journal of Advanced Research in Computer Science
RESEARCH PAPER
Available Online at www.ijarcs.info

Redundancy for Fault Tolerance Algorithm in FPGA Architecture for Reliability with a BIST Approach

Ms. Shweta S. Meshram*
Electronic and Telecommunication Department
Government College of Engineering & Technology
Amravati, India
Shwt.meshram@gmail.com

Ms. Ujwala A. Belorkar,
HOD of Electronic Department
HVPM's College of Engineering & Technology
Amravati, India
ujwalabelorkar@rediffmail.com

Abstract: In recent years the application space of reconfigurable devices has grown to include many platforms with a strong need for fault tolerance. The decreasing feature sizes resulting from the improvement in the fabrication techniques has resulted in chips with very high device count. Redundancy based hardening techniques are applied at the pre-synthesis or synthesis level. To provide solutions for increasing the fault-tolerance capabilities with algorithms able to reduce sensitive configuration memory bits of FPGAs we use BIST method. If nano-technology fabrication are applied the yield may go down to zero as avoiding defect during fabrication will not be a feasible option Hence, feature architecture have to be defect tolerant. We presented a new approach for testing FPGA's by utilizing their reprogrammability. It gives solution in which configuration bit-stream of FPGA is modified by a hardware controller with BIST that is present on the chip itself.

Keywords: Redundancy, Fault Tolerance, FPGA, Altera, BIST, Defect.

I. INTRODUCTION

The occurrence of defects during manufacturing is a random process. While data exist regarding the density and clustering of defects, it is impossible to formulate prediction models regarding the location of the defects within a die. As such, the probability of obtaining even two defective devices which exhibit the same functional fault in exactly the same location is almost non-existent. As FPGAs continue their expansion into the semiconductor market, they are more and more often utilized in medium volume products. One of the biggest challenges offered by fault tolerance is therefore ensuring that the same bitstream produced can be successfully matched to tens, hundreds, and potentially even thousands of non-identical devices.

VLSI technology progress for finer dimension and larger chip area has lead to more complex process and introduction of new and more complex material system [1]. Due to higher defect density and complicated fabrication technique the cost of manufacturing has increased. The increase in defect/fault complexity factor has lead to more devices being effective and hence reduced the yield. Researches for improving yield using various techniques are being carried out since many years [4]. Without using redundancy, the reliability of system is limited by the reliabity of its components. Moreover the system is unprotected from transient errors. Adding fault tolerance to design to improve the dependability of system requires the use of redundancy i.e. One of the ways to achieve higher yield is use of fault tolerance [3]. Incorporating fault tolerance in architecture allows us to use the chip even if a chip is faulty. In this paper we propose a new FPGA like architecture which incorporate fault tolerance in the fabric.

Various defects may be produced in a VLSI chip during manufacturing [2]. The existence of defects affects yield and ultimately cost. Field programmable gate arrays (FPGAs) are especially expensive because of the large area penalty taken in favors of reconfigurability. With advancement in process technology, the feature size is decreasing which leads to higher defect densities more sophisticated techniques at increased costs are required to avoid defects.

If nano-technology fabrication are applied the yield may go down to zero as avoiding defect during fabrication will not be a feasible option Hence, feature architecture have to be defect tolerant. In regular structure like FPGA, redundancy is commonly used for fault tolerance [5]. In this work we present a solution in which configuration bit-stream of FPGA is modified by a hardware controller that is present on the chip itself [6]. The The technique uses redundant device for replacing faulty device and increases the yield. The design is implemented using FPGA Altera Quartus II [8].

II. PRELIMINARIES

There are two major approaches to deal with fault tolerance in FPGA. First is Software based approach where the fault map is given as input to place and route tool and generated configuration does not use the cell which are faulty. Another approach is Hardware based in which configuration bit-stream generated by Software is modified by Hardware [7]. Our technique is also Hardware based but we assume that FPGA to be fault free. In another work, fault tolerance is studied at interconnect level and also column based redundancy which is more useful for less number of defect [5].

III. PROPOSED TECHNIQUE

In this paper, we are proposing a technique in which a hardware controller on the FPGA takes defect map and configuration file as input & outputs the modified configuration file. We are also using spare device for defect tolerance. If we find any defect in FPGA than the spare device is used and discard the faulty device. The proposed technique is unique because the configuration bit-stream is modified by Hardware not by Software.

The defect map is generated by BIST (built in self test) which is off line Structural type of BIST, present on the chip. Each chip will have different defect map. In some cases fault can also occur after the chip has been manufactured and tested. In our approach the fact that we modify the configuration bit stream in Hardware inside the chip rather than software allow us to handle such faults [2].

Process variations and complex fabrication techniques are one of the factors responsible for producing defects in the final chip. In this section, we first elaborate on the fault model that we have used to propose a method which exploits the increased device density to provide fault tolerance to the FPGA fabric. Thus allows us to use "partially defective" FPGA chips. We are proposing a technique in which a hardware controller on the FPGA takes defect map and configuration file bit stream as input and outputs the modified configuration file. We are also using spare columns for defect tolerance. If we find any defect in the FPGA then the spare column is used, discarding the faulty column. The spare column which are use are called Redundancy.

IV. FAULT AND DEFECT MODEL

Fault is that defect which affects the circuit operation [1]. There are two types of defects present in the wafer, global defect & spot defect. Global defect affect larger area of the chip, on other hand spot defect are completely random in nature and can occur anywhere on the chip and can cause short or open in the wire. In this paper we consider only faults which occur due to spot defect in the FPGA [3].

A. System Architecture

System Architecture consist of three models 1) Testing Circuit 2) Configuration Control 3) Fault Controller. Figure 1 show the flow of configuration of a faulty FPGA with the fault tolerant technique. Two new hardware blocks are present on the chip, one is the testing circuit which check faulty device in the FPGA and generate fault map. Another is the fault controller that argument configuration bitstream to generate a new bit-stream with the help of fault-map [7].

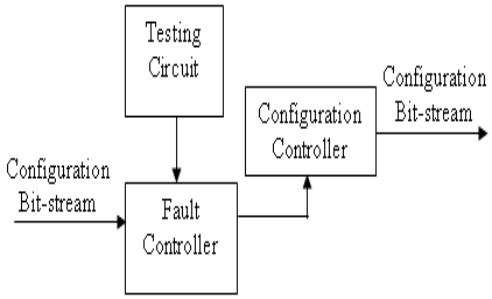


Fig.ure 1. Configuration Flow

If a device found faulty, fault controller generate another configuration in which the faulty device in not used and it is shifted to the spare device.

B. Build In Self Test

Built in Self Test is the capability of a circuit (Chip, Board, or System) to test itself. BIST represents a merger of the concepts of built-in test and self test. BIST technique can be classified into two categories

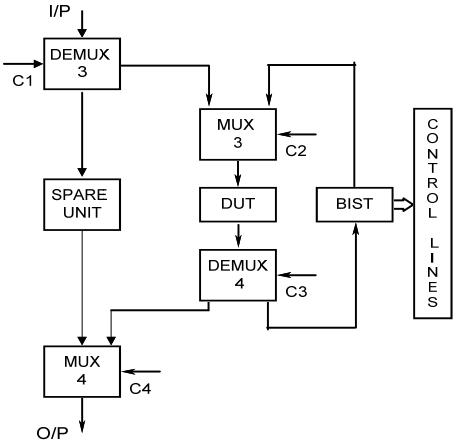
1) On Line BIST 2) Off Line BIST

On line BIST, includes concurrent and non concurrent techniques and Off line BIST, includes functional and structural approaches. In on line BIST, occurs during normal functional operation conditions. Concurrent on line BIST is a form of testing that occurs simultaneously with normal functional operation. In non concurrent on line BIST, testing is carried out while a system is in idle state.

Off line BIST deal with testing a system when it is not carrying out its normal functions. System, board and chips can be tested in this mode. Functional Off line BIST deals with the execution of a test based on a functional description of the testing circuit. Structural Off line BIST deals with the execution of a test based on a structural description of the testing circuit.

C. Hardware Controller

Figure 2 show the architectural view of fault tolerance in FPGA architecture, in this we design a device, which is put in Device under Test (DUT) & also kept one spare device, assuming that the spare device is fault free.



Cl, C2, C3, C4- Control Lines

Figure. 2. Block Diagram of Hardware Controller

D. Proposed Algorithm

Step 1: Send/make control signal so that the DUT of BIST route created and along with disconnect the DUT from practical use and send Busy signal at the external world.

Step 2: Place one defined set of pattern on the DUT to test.

Step 3: Get the output pattern.

Step4: Compare the output pattern with the expected result.

Step 5: If output is OK discarding the remaining step and connect DUT for normal use.

Step 6: If result is not matching, than it state that DUT is faulty.

Step7: Discard DUT and replaced by Spare Unit and get desire output pattern.

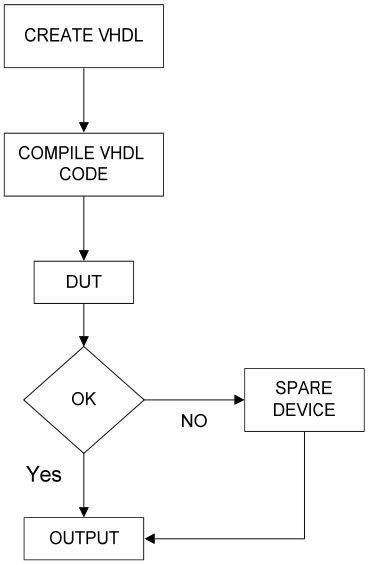


Figure 3. Flowchart

V. SIMULATION RESULT

A. *Decoder*

We design DECODER with input A, B and SEL. If DUT is faulty free then faulty signal became low and give desire output. Following waveform shows the fault free working of decoder with the help of device under test.

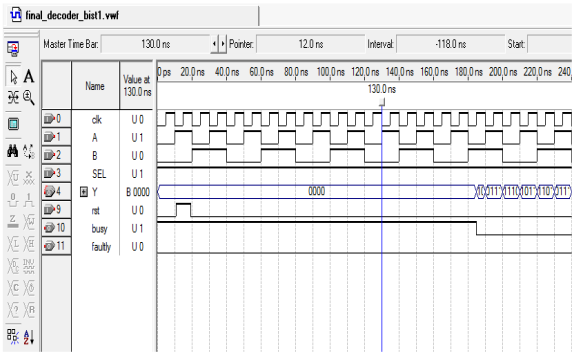


Figure 4. Simulation result of decoder with no Fault

If there is fault in DUT than faulty signal will be high and DUT is replaced by spare unit which is assume to be fault free and give desire output.

Following waveform shows the fault free working of decoder with the help of spare device as device under test is faulty.

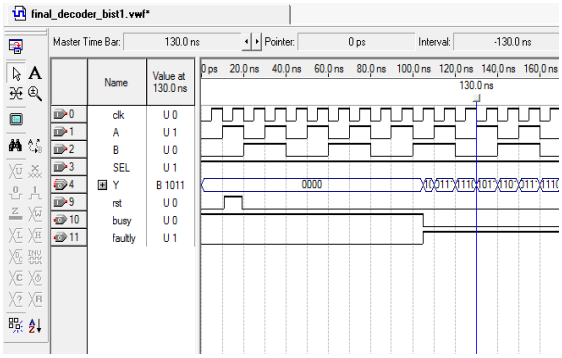


Figure 5. Simulation result of decoder with Fault

B. *Mux*

We design Mux2:1 with input A= 00000001 and B= 00000011.As we select Sel line Sel = 0, the output will be A i.e. 00000001. And if we select Sel = 1, then output is B i.e. 00000011.Since the designed Mux is fault free, faulty signal became low.

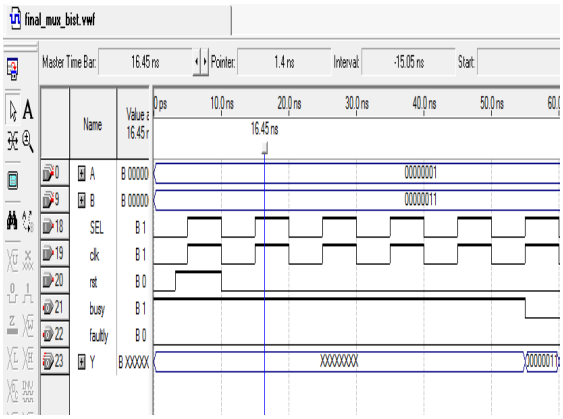


Figure 6. Simulation result of mux with no Fault

In figure 7 simulation result as the device is faulty, we get the output from the spare device. Simulation result indicates device under test is faulty and faulty signal became high.

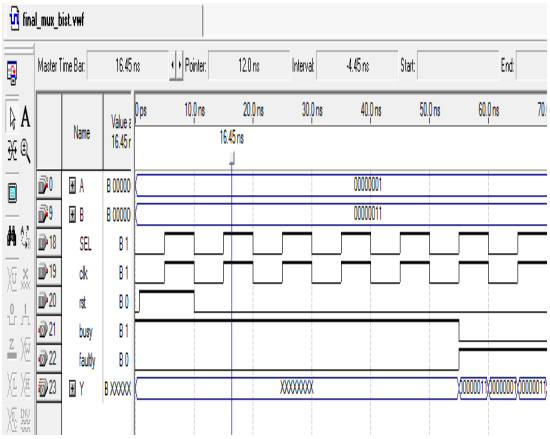


Fig. 7 Simulation result of mux with Fault

C. *Adder*

For designing Adder with input A = 00001100 and B = 10001010, the output became Y = 010010110. Since the designed Adder is fault free, faulty signal became low.

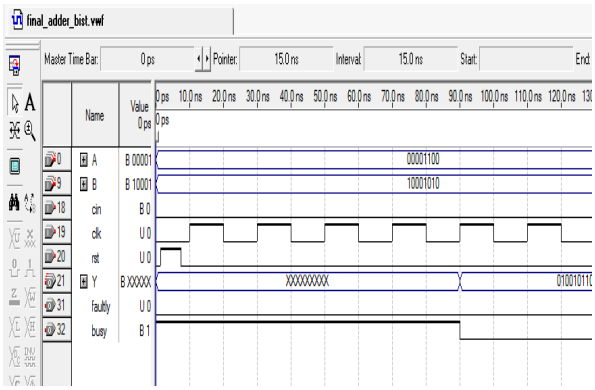


Figure 8. Simulation result of adder with no Fault

In this simulation result as the device is faulty, we get the output from the spare device. Simulation result indicates device under test is faulty and faulty signal became high.

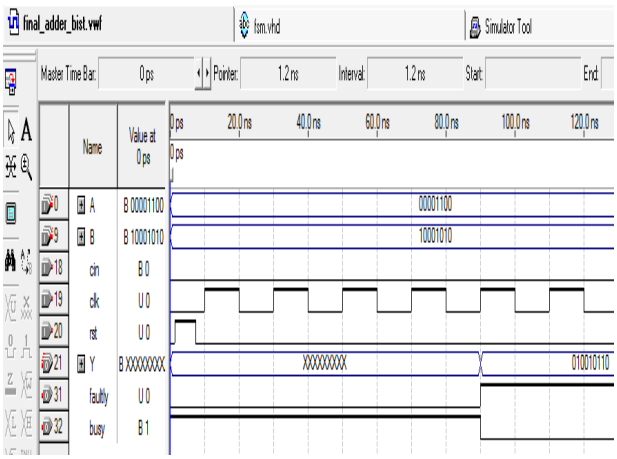


Figure 9. Simulation result of adder with Fault

Table 1: Device with Hardware Controller

Device Under Test	Logic Element	Power Dissipation	Time delay
Decoder	24	30 mW	0.12ns
Mux	24	25 mW	0.21ns
Adder	67	34mW	0.14ns

.

VI. YIELD ANALYSIS

In this section, we analyses the effect of yields on the performance of systems built using our approach. We have presented a simple scheme that facilitates defect tolerance in FPGA systems. Using defective FPGAs can substantially drive down the cost of the system. Our analysis of success probability shows that large systems with high degrees of symmetry can appear nearly the same as defect-free systems. The only trade-off may be the cost of extra units required in circuit. Nevertheless with careful design of the system, the right balance between symmetry and implementation cost can be determined, and significant cost savings can be realized so as to increase in yield. We feel that defect tolerance must be considered as one of the key factors in determining a cost benefit to implementing the application on FPGA.

VII. CONCLUSION

With advance in process technology, the feature size is decreasing which leads to higher defect densities. This design approach present a novel Hardware controller based mechanism for fault tolerance in defective FPGA. By this approach we can use the device even it is found faulty. The method can be used by FPGA vendor to increase yield & thus decrease the cost. In this propose work we have given detailed designed algorithm for the fault controller. This work enables us to look in a different paradigm of circuit design where faults in a chip are handled by the circuit inside the chip itself using redundancy.

The proposed method affects three aspect yield, area of chip & delay. By this approach we get the maximum (100%) yield whereas area is concern, as we are using spare device area will increase and due to increase in area the affect time delay of various nets

V. REFERENCES

[1] H. Sewell, D. McCafferty, L. Markoya, E. Hendrickx, J. Hermansand, and K. Hermans. 32nm node technology development using interference immersion lithography. Proceedings of the SPIE, 5753:491–501, 2005.

[2] N. Campregher, P. Cheung, G. Constantinides, and M. Vasilko. Analysis of yield loss due to random photolithographic defects in the interconnect structure of fpgas. In FPGA, 2005.

[3] Koren and Z. Koren. Defect tolerance in VLSI circuits: Techniques and yield analysis. Proceedings of the IEEE, 86(9), Sept 1998.

[4] F. Hatori, T. Sakurai, K. Nogami, K. Sawada, M. Takahashi, M. Ichida, M. Uchida, I. Yochii, Y. Kawahara, T. Hibi, Y. Saeki, H. Muroga, A. Tanaka, and K. Kanzanki. Introducing redundancy in field programmable gate arrays. In Custom integrated Circuis Conference, 1993.

[5] W. J. Huang and E. McCluskey. Column based pre-compiled configuration technique for fpga fault tolerance. In FPGA, 2001

[6] A. J. Yu and G. G. F. Lemieux. Defect tolerant fpga switch block and connection block with fine grain redundancy for yield enhancement. In IEEE International

Conference on Field Programmable Logic and Applications, 2005.

[7] S. Mitra, P. Sirvani, and E. McCluskey. Fault location in fpga based reconfigurable systems. In IEEE Intl High Level Design Validation and Test Workshop, 1998.

[8] M. Naseer, P.Sharma, R. Kshirsagar. Fault Tolerance in FPGA Architecture Using Hardware Controller - A Design Approach. In International Conference on Advances in Recent Technologies in Communication and Computing, 2009.

VI. ACKNOWLEDGMENT

The authors would like to thank the reviewers for providing very detailed comments.

VII. AUTHORS

Short Biography

Ms. Shweta S. Meshram was born in Amravati, Maharashtra in 1988. She is pursuing the M.E. Degree in Electronics System and Communication from S.G.B. Amravati University. Her research focuses mainly on applying optimization techniques and designing parallel algorithms for VLSI physical design problems, particularly algorithms for placement and routing and Micro Electronic System Design using VLSI Technology & VHDL based FPGA design.

Ms. Ujwala A. Belorkar was born in Amravati, Maharashtra in 1970. She received the M.E. Degree in Digital Electronics from S.G.B. Amravati University, Amravati in 2004 & pursuing Ph.D. Degree in Electronics Engineering. Currently she is working as a Assistant Professor & Head in Electronics & Telecommunication Department at H.V.P.M's College of Engineering & Technology, Amravati. Also she is working as a visiting faculty for M.Tech. in Advanced Electronics at Govt. College of Engineering Amravati. She is the editorial board member for international journal on VLSI & communication system. Her interests are in Micro Electronic System Design using VLSI Technology.