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Memory Circuit Design in Quaternary Logic

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Abstract— The most widely used semiconductor memory types are the Dynamic Random Access Memory [DRAM] and Static Random Access memory (SRAM). Competition among memory manufacturers drives the need to increase the storage capacity per chip and reduce the cost per bit. A technology that has not been successfully exploited commercially is the Multilevel DRAM [MLDRAM], which offers lower cost-per-bit without the expense of retooling the DRAM manufacturing process. MLDRAM differs from conventional DRAMs by storing more than one bit per storage cell. This paper proposes and analyses a new MLDRAM sensing scheme and also analyses SRAM single cell. The accuracy of the result is validated by means of Hspice simulations with 90nm and 50nm technology to explore the applicability of the results in deep submicron technologies.

Keywords: — DRAM, SRAM, MLDRAM, Multi-valued logic, Sense amplifier

I INTRODUCTION

Multi-valued logic circuits increase the capacity of single line carrying information, resulting in improving the information density of digital circuits, reducing the area and pin-count of integrated circuit chip. So research workers have played great attention on it [1-3]. However, the present multi-valued logic circuits use binary components, its structures are complexly compared with binary circuits which have the same function, resulting in high-power consumption. So it is more important to explore low-power design of multi-valued logic circuits [4].

A. DRAM

Multiple-Valued DRAM is useful in many applications such as neural networks [5]–[10], where a massive number of values has to be stored on the chip. Multiple-Valued memories have the ability to increase the bits-per-cell storage capacity by storing more than one bit of information on each memory cell [5]–[10], [11]–[18]

Birk et al. [13, 21] proposed an inherently robust MLDRAM that combines the speed advantages of paper[17] with the noise cancellation advantages of paper[16]. This paper describes an MLDRAM test chip that is more flexible than Chan' s 2-bit-per-cell implementation of Birk' s MLDRAM [21]. The test chip, which is being simulated and laid out in TSMC' s 180 nm CMOS technology, can be operated either as a conventional 1-bit-per-cell DRAM or as a 1.5, 2 or 2.5-bits-per cell MLDRAM. Regardless of the selected cell capacity, data storage and sensing follow the same mechanisms described in [13]. Thus the results of sensing parallel cell arrays are combined to give the recovered binary data. The ability to adjust the cell capacity will be useful for characterizing test chip and for experimentally determining the practical limits of one particularly promising MLDRAM technology [22].

M. Aoki proposed a 4-bit per cell multilevel sense and restore technique. The basic operation of the scheme is timed to a staircase pulse that is applied to the selected word line. Data to be written is stored in a special register in the column. Data is written into the cell as one of sixteen voltage levels by synchronizing the staircase word line signal to the write circuitry controlled by the column register. When the word lines begin descending, the bit lines are set to 0 Volts. The column register, carrying a data value i, causes the bit line to rise from 0 V to V_{DD} during the i-th step of the descending word line voltage. The n-channel cell access transistor allows current to flow from the raised bit line into the cell until the cell voltage is equal to one threshold voltage below the word line voltage. Thus raising the bit line voltage during the appropriate step interval of the descending word line chooses one of sixteen levels. Data is read from the cell by applying an ascending staircase to the word line. For a cell that contains voltage level i, the bit line will first be disturbed when the word line reaches voltage level i+l. To sense the small voltage, pre-amplifiers are placed in the bit line pitch, the outputs of the pre-amplifiers are fed to a bit line sense amplifier. The time when the sense amplifier detects the first disturbance on the bit line determines the read value according to the current state of the word line staircase clock. Data may be read or written to the column register prior to the write operation, which restores the correct signal voltage to the cell. This scheme has the advantage of being scalable to any number of levels [19].

The main disadvantage of Furuyama's MLDRAM scheme is that it is susceptible to sensing errors due to improper reference values. The potential for such errors arises from the use of global reference voltages that need to be generated on chip and distributed across the array. A slight inaccuracy in the global reference voltage levels would be enough to cause sensing errors [17].

The major advantage of Gillingham's MLDRAM compared to previous MLDRAM schemes is that this scheme uses local components to generate the reference voltages, rather than special reference cells and power supplies. Another redeeming quality is that the circuit is composed of proven standard DRAM sub-circuits. There are no special capacitors or cells. Thus the departure from proven techniques is limited to the operational and configuration of

proven core circuits rather than the optimized cell array [16].

The main advantage of Okuda's [4] MLDRAM scheme is its simplicity. The extra circuitry needed is minimal and the control timing is relatively simple. The most vulnerable aspect of this design is the use of the coupling capacitors to produce the LSB reference. These capacitors must be exactly proportionated to the cell capacitance since any error in the ratio translates directly into a reduction in the noise margins. This makes the design susceptible to processing deviations. As well, there may be some error associated with the uneven partitioning of the bit line into sub-bit lines that are related by a parasitic rather than geometrical symmetry [14].

B. SRAM

The read/write (R/W) memory circuits are designed to permit the modification (writing) in the memory cell, as well as their retrieval (reading) on demand. The memory circuit is said to be static if the stored data can be retained indefinitely (as long as sufficient power voltage is provided), without any need for a periodic refresh operation. The data storage cell or the 1-bit memory cell in static RAM, invariably consists of a simple latch circuit with stable operating points (states). Depending on the preserved state of the two-inverter latch circuit, the data being held in the memory will be interpreted as logic '0', '1', '2' or '3'. To access (read or write) the data contained in the memory cell via the bit line, we need at least one switch. Two complementary access switches consisting of nMOS pass transistors are implemented to connect the 1-bit SRAM cell to the complementary bit lines (columns).There are many configurations of a SRAM.

Resistive-load inverter latch SRAM cell: The use of resistive-load inverters with undoped polysilicon resistors in the latch structure typically results in a significantly more compact cell size. In order to attain acceptable noise margins and output pull-up times for the resistive-load inverter, the value of the load resistor has to be kept low. On the other hand, a high–valued load resistor is required in order to reduce the amount of standby current being drawn by each memory cell. Thus, there is a trade-off between the high resistance required for low power and the requirement to provide wider noise margins and high speed.

Depletion-load nMOS SRAM cell: The six-transistor depletion-load nMOS can be implemented with one polysilicon and one metal layer, and the cell size tends to be relatively small, especially with the use of buried metal-diffusion contacts.The static characteristics and the noise margin of this memory cell are typically better than those of the resistive-load cell.The static power consumption of the depletion-load SRAM cell, however, makes it unsuitable for high density SRAM arrays.

C. CMOS SRAM cell

The full CMOS SRAM cell is the most popular due to lowest static power dissipation among the various configurations and compatibility with current logic process.In addition, the CMOS cell offers superior noise margins and switching speed as well.The possible drawback of using CMOS SRAM cell is that the cell area tends to be slightly larger in order to accommodate the n-well for the pMOS transistors and polysilicon contacts.

Since much of work on multi-valued SRAM has not been carried out so for, we have discussed more about binary SRAM in the above section.

II. MLDRAM CHALLENGES

MLDRAM offers a great increase in memory density by storing multiple bits per cell. However, this increase in density comes with a price. One major penalty that is incurred is the reduction in noise margins. For example, a four level (2 bit) MLDRAM will have noise margins that are 1/3 as big as those of standard DRAM. With today's low voltage supplies; the use of more than four levels would make the noise margins extremely low. For this reason, this paper will focus on four levels DRAM.

These noise margins become even more important due to the inherent charge leakage problem with DRAM. Due to sub-threshold conduction in short-channel MOSFETs, the charge on a memory cell capacitor leaks onto the data line. With large noise margins, this problem is not as important because more charge can leak before the value on the capacitor changes from a "1" to a "0". However, as the number of voltage levels is increased, and the supply voltage is decreased, the amount of charge that can safely leak from a memory cell decreases dramatically.

Another problem with MLDRAM is that the sense and restore technique becomes more complex. With standard DRAM one voltage value is decoded into one bit. However, with MLDRAM one analog voltage value must now be converted into two bits of information. This new level of complexity leads to increased access times, increased energy usage and a smaller increase in density than expected due to increased peripheral circuitry.

A. MLDRAM technology

It is becoming increasingly expensive to raise the storage density of DRAM by reducing the physical size of the cell. One additional dimension, which has yet to be successfully exploited in commercial parts, is to store more than one bit per cell. In a DRAM cell this involves storing and then subsequently sensing more than two distinct voltage levels on the cell capacitor. In DRAM, the cell voltage can be defined as one of two possible values (Equation 1.1).

$$V_{cell} \in \{a_0, a_1\}, \text{ where } 0 \le a_i \le 1 \qquad (1.1)$$

In MLDRAM, the number of allowed states N is greater than two. N is related to the number of bits (n) by equation 1.2.

$$N=2^n \qquad (1.2)$$

Thus, for n-bit storage the allowed cell voltages are:

$$V_{cell} \in \{a_0, a_1, a_2, a_3 \ldots a_{N-1}\} (V_{DD}) \qquad (1.3)$$

The coefficients a_i should be chosen to maximize the noise margins between them. This can be achieved if the allowed voltages in the cell are equally spaced in the available voltage range as follows:

$$V_{cell} \in \{0, 1, 2 \ldots\ldots N-1\} (V_{DD})/N-1 \qquad (1.4)$$

To read the multilevel data, the cell voltage is compared to a set of reference voltages. There is one reference voltage between each allowed cell voltage. The N-1 reference voltages (V_{ref}) are equally spaced between the possible cell voltages (V_{cell}) to give equal and maximum noise margins between all references and cell voltages. The reference voltages are given in Eq. 1.5.

$$V_{ref} \in \{1, 3, 5 \ldots\ldots 2N-3\} (V_{DD})/2(N-1) \qquad (1.5)$$

Table 1 shows binary reference voltage, cell voltage and logic levels. Table 2 illustrates an example of how one might encode the four logic pairs 00, 01, 10 and 11 as four equally-spaced voltage levels in the range $V_{SS} = 0$ to V_{DD}. The cell voltages must be compared to the reference levels to extract two bits from a cell. If the cell voltage is less than $^1/_6V_{DD}$ then the value of the bits is 00. If the cell voltage is greater than $^1/_6V_{DD}$ but less than $^1/_2V_{DD}$ then the value of the bits is 01, and so on.

Table I: binary voltage levels

Conventional		
Ref. voltage	***Cell voltage***	***Binary***
	V_{DD}	1
$V_{DD}/2$		
	V_{SS}	0

Table II: Quaternary voltage levels

Multilevel		
Ref. voltage	***Cell voltage***	***Binary***
	V_{DD}	11
$^5/_6V_{DD}$		
	$^2/_3 V_{DD}$	1 0
$^1/_2 V_{DD}$	$^1/_3 V_{DD}$	0 1
	V_{SS}	0 0

B. Concept of multiple sensing

Sensing multiple levels in MLDRAM is of two ways. It can be parallel sensing or sequential sensing. Both schemes have their own advantages & disadvantages. This section introduces both the sensing schemes.

a. *Parallel sensing:* Two schemes have been proposed for parallel sensing of multi-level data. The two schemes are similar in many ways except for the method in which they generate their reference voltage. One of the schemes uses a globally generated reference voltage, and the other uses a locally generated reference voltage.

During standby, all bit lines are charged to $V_{dd}/2$. For a read cycle, the value stored in the cell is read onto the bit line. Transmission gates into three separate sub-bit lines which make up blocks A. B, and C then separate the bit line. After separation, each of the sub-bit lines should have the same potential as the original cell and should be connected to a given sense amplifier. For reference, three equally spaced global reference voltages are written to dummy memory cells in each block such that now, each block has its own reference voltage.

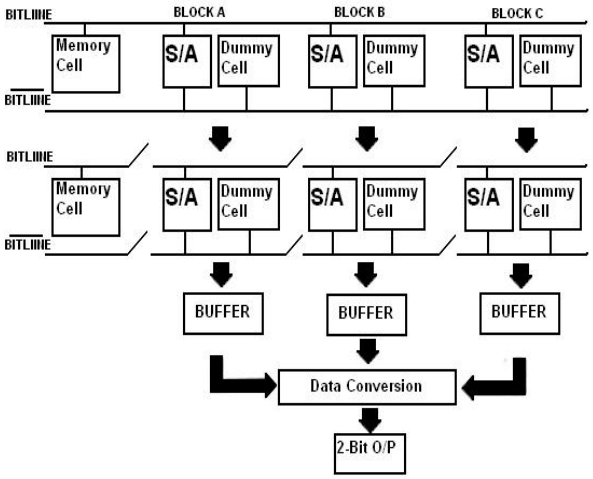

Figure 1: Parallel sensing scheme using globally generated reference voltage.

Through the complement sub-bit lines, each of these reference voltages is used as an input to a sense amplifier to determine if the value on each of the sub-bit lines is greater or less than the reference voltage. If the sub-bit line value is greater than the reference voltage, the sense amplifier will output a "1"; otherwise it will output a "0". The three sense amplifier outputs are then sent to a buffer and converted to two binary bits. Table 3 lists the cell voltages, the reference voltages, the binary output of the sense amplifiers, and the final binary output bits are converted into three and the resulting values are placed in their respective blocks.

Table III: Voltage and binary values for parallel sensing.

Cell Voltage	***Reference Voltage***	***S/A Binary Output***	***Final Binary Output***
Vdd		111	11
	5Vdd/6		
2Vdd/3		011	10
	Vdd/2		
Vdd/3		001	01
	Vdd/6		
Gnd		000	00

When the transmission gates are closed, charge sharing occurs and the resulting value on the overall bit line is placed in the memory cell. For example, if "01" is converted to "001", blocks A and B will receive a 0 value (ground), and block C will receive a value of V_{dd}. When the sub-bit lines are connected, the charge equalizes to $V_{dd}/3$. This value is then placed in the memory cell.

The second parallel sensing technique uses many of the same ideas as above, but creates the reference voltages local to these sense amplifiers.

b. *Sequential Sensing:* Like the parallel sensing method, there are two main methods that have been developed and tested for sequential sensing of data in MLDRAM. The main difference between the two methods is in how they produce their reference voltages. One method uses charge sharing and a transistor switch matrix connecting multiple sub-bit lines to create reference voltages while the other method uses capacitive coupling between sub-bit lines. In addition to these two techniques, a third

scheme that uses a sequential staircase voltage to insert data to and extract data from the memory cell.

IV Circuit Description Of Proposed Multilevel Sense Amplifier

Sequential sensing scheme is adapted in the proposed method. This method consists of two sense amplifiers, one for sensing MSB bit and other to sense LSB bit.

To achieve read time of 6.65ns, ratio $(W/L)_n = 3$ and $(W/L)_p = 7.5$ are chosen. Thus for nmos L=100nm, W=300nm and for pmos L=100nm, W=750nm are used in the circuit design.

A. Circuit operation

The circuit diagram of the proposed multilevel sense amplifier using sequential scheme is as shown in figure 2. To start with, the reference voltage for sense amplifier A is a constant and always set to $V_{dd}/2$. Whereas the reference voltage for sense amplifier B is generated locally from sense amplifier A. voltage on bit line of sense amplifier A itself is reference voltage for sense amplifier B.

The proposed scheme is able to sense four levels. The voltage levels in storage capacitor of DRAM cell for four levels are as shown in table 3.

As explained previously, proposed sense amplifier serves the purpose of sensing two bits per cell. The detailed operation of sensing all the four levels is explained in case 1, case 2, case 3 and case 4.

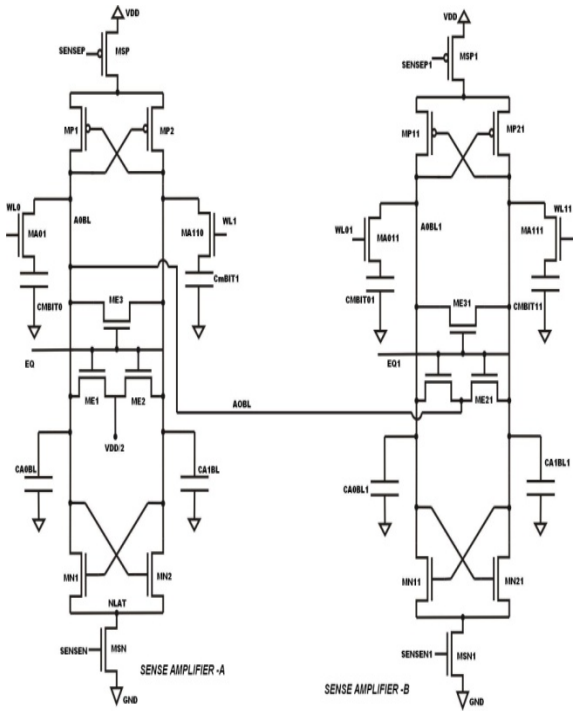

Figure 2: Proposed multilevel sense amplifier using sequential scheme.

Table IV: Voltage levels sensed by multilevel sense amplifier.

Voltage Level	*Binary Value*
V_{dd}	1 1
2/3 V_{dd}	1 0
1/3 V_{dd}	0 1
Vss	0 0

CASE 1: Cell voltage is V_{dd}

If the voltage across storage cell is V_{dd} (1V), the bits to be sensed are 1 1. Since the reference voltage of sense amplifier A is set to 0.5V and storage cell voltage is of 1V, the bit line of sense amplifier is pulled to V_{dd} (logic 1).

Bit line of sense amplifier A is connected to sense amplifier B and serves as reference voltage to sense amplifier B as shown in figure 2. Since the reference voltage of sense amplifier B is set to 1V and storage cell voltage is of 1V, the bit line of sense amplifier B is pulled to V_{dd} (logic 1). Hence the bits stored are predicted as 1 1. The Hspice simulation result for CASE 1 is shown in figure 3. Circuit is designed for read time of 6.65ns.

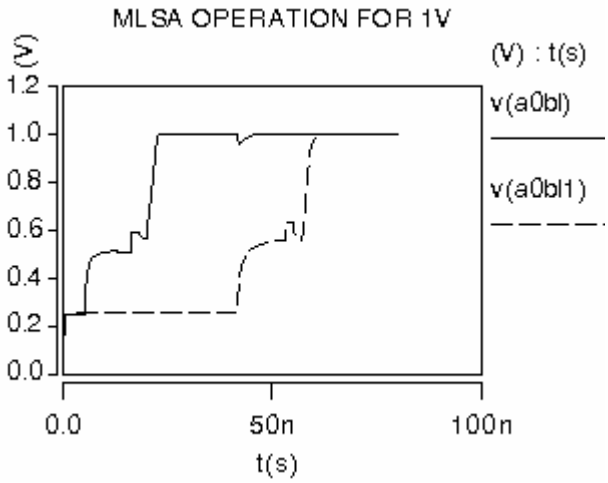

Figure 3: Result analysis for CASE 1.

The power dissipation is measured using the Hspice tool and the dynamic power, for CASE 1, is found to be 40.992µW and the static power is found to be 1.2277 µW at 90nm technology and dynamic power of 17.026 µW, static power of 1.3537 µW for 50nm technology.

CASE 2: Cell voltage is 2/3 V_{dd}

If the voltage across storage cell is $2/3V_{dd}$ (0.66V), the bits to be sensed are 1 0. Since the reference voltage of sense amplifier A is set to 0.5V and storage cell voltage is of 0.66V, the bit line of sense amplifier is pulled to V_{dd} (logic 1). This voltage level serves as reference voltage to sense amplifier B. Since the reference voltage of sense amplifier B is set to 1V & storage cell voltage is of 0.66V, the bit line of sense amplifier B is pulled to Vss (logic 0). Hence the bits stored are predicted as 1 0. The Hspice simulation result for CASE 2 is shown in figure 4.

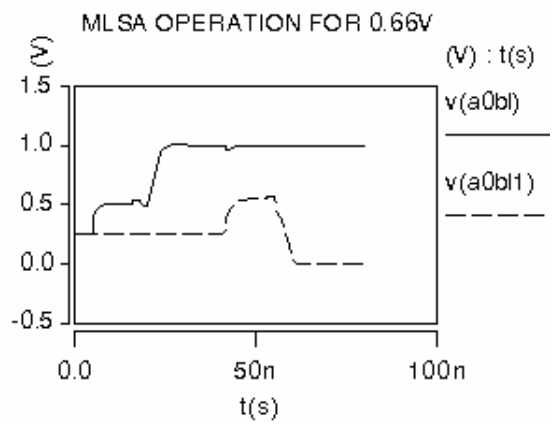

Figure 4: Analysis for CASE 2.

Dynamic power, for CASE 2, is found to be 29.093 µW and the static power is found to be 1.2494 µW at 90nm technology and dynamic power of 15.466 µW, static power of 1.5506 µW for 50nm technology.

CASE 3: Cell voltage is 1/3 V_{dd}

If the voltage across storage cell is $1/3V_{dd}$, the bits to be sensed are 0 1. Since the reference voltage of sense amplifier A is set to 0.5V & storage cell voltage is of 0.33V, the bit line of sense amplifier is pulled to V_{ss}, i.e. logic 0.

Hence the coupling capacitor gets charged to V_{ss} & serves as reference voltage to sense amplifier B. Since the reference voltage of sense amplifier B is set to 0v & storage cell voltage is of 0.33v, the bit line of sense amplifier B is pulled to V_{dd} i.e. logic 1. Hence the bits stored is predicted as 0 1. The Hspice simulation result for CASE 3 is shown in figure 5.

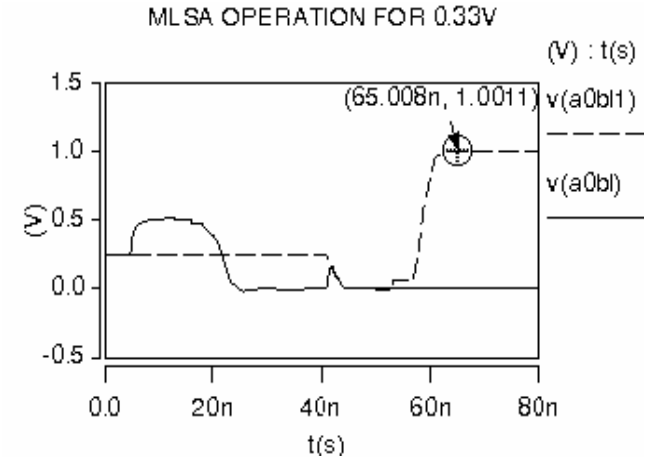

Figure 5: Analysis for CASE 3.

Dynamic power, for CASE 3, is found to be 64.049 µW and the static power is found to be 1.8916 µW at 90nm technology and dynamic power of 35.084 µW, static power of 2.3710 µW for 50nm technology.

CASE 4: Cell voltage is V_{ss}

If the voltage across storage cell is V_{ss}, the bits to be sensed are 0 0. Since the reference voltage of sense amplifier A is set to 0.5V and storage cell voltage is of 0V, the bit line of sense amplifier A is pulled to V_{ss} (logic 0). This voltage level serves as reference voltage to sense amplifier B. Since the reference voltage of sense amplifier B is set to 0V and storage cell voltage is of 0V, the bit line of sense amplifier B is pulled to V_{ss} (logic 0). Hence the bits stored are predicted as 0 0. The Hspice simulation result for CASE 4 is shown in figure 6.

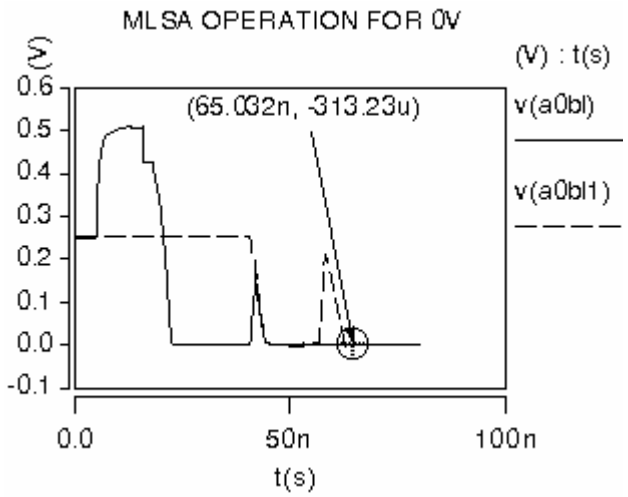

Figure 6: Analysis for CASE 4.

Dynamic power, for CASE 4, is found to be 69.419 µW and the static power is found to be 2.1127 µW at 90nm technology and dynamic power of 35.456 µW, static power of 2.2528 µW for 50nm technology.

The MLSA, proposed and simulated in this paper has numerous advantages. Advantages of this Multi-Level Sense Amplifier over other sense amplifiers are as follows: Sequential sensing of MSB and LSB, No requirement of reference voltage generation, Fast read access, Two sense amplifiers are sufficient for sensing two bits per cell, Very less consumption of area. These advantages can be made use of in the current scenario where slow but steady research is underway to develop and shift to multi-level logic circuits including memory circuits that can hold more than one bit per cell.

V SRAM DESIGN

A. Quaternary Static Random Access Memory Cell

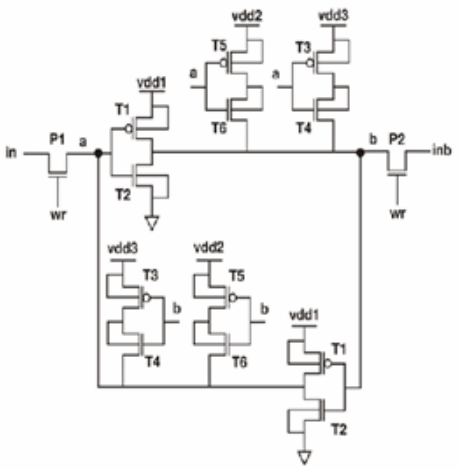

Figure 7: Gate level representation of Quaternary SRAM cell.

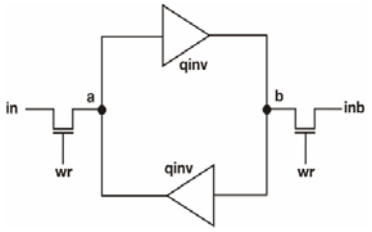

Figure 8: Block diagram representation of SRAM cell.

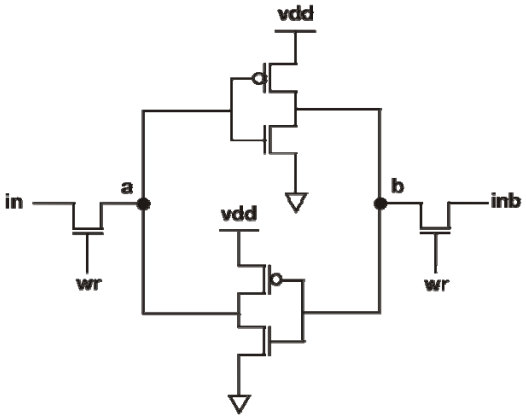

Figure 9: Circuit diagram representation of binary SRAM cell.

A. Design Strategy

The quaternary SRAM cell is shown in figure 7 and figure 8 respectively. Let us consider the gate level implementation. We have designed it by using cross-coupled CMOS quaternary inverters acting as a latch.

The two basic requirements which dictate the (W/L) ratios are: The data-read operation should not destroy the stored information in the SRAM cell. The cell should allow modification of the stored information during-write phase.

Consider the data-read operation, assuming that logic '0' is stored in the cell: Here, the transistors "T1" on top row and "T2" from bottom row operate in linear mode. Other transistors are turned off. Thus, the internal node voltages are V_a = '0' and V_b = 'vdd1'. During the read operation in a SRAM array, the access transistors are "on" , which leads to discharging of column capacitance, leading to node voltage increase from initial value of '0' V. If the (W/L) ratio of the access transistor 'P1' is large compared to the (W/L) ratio of 'T2' of bottom row, the node voltage V_a may exceed the threshold voltage of "T2" of top row during this process, forcing an unintended change of the stored value.

The key design issue for the data-read operation is then to guarantee that the voltage V_a does not exceed the threshold voltage of "T2" of top row , so that it remains turned "off" during the read phase ,i.e.,

$$Va,max \leq Vt,2 \quad \text{.....} \quad (1)$$

After the access transistors are turned on, the column voltage remains approximately equal to vdd1. Hence, "P1" operates in saturation while "T1" operates in linear region. Thus,

$$\frac{\frac{W}{L}_{P1}}{\frac{W}{L}_{T2}} < \frac{2(Vdd - 1.5Vt,n)Vt,n}{(Vdd - 2Vt,n)^2} \quad \text{.....} \quad (2)$$

To summarize, the transistor "T2" of bottom row will remain in cut-off during the read '0' operation, if equation 2 is satisfied. A symmetrical condition also dictates the aspect ratios of other transistors.

Now, consider the write '0' operation, assuming that logic '3' is stored in the SRAM cell initially. The transistors "T1" of bottom row and "T2" of top row operate in linear mode. Thus, the internal voltages are V_a= 'vdd1' and V_b = '0' before the cell access transistors "P1" and "P2" are turned "on". To change the stored information, It means to force V_a to '0' V and V_b to "vdd1", the node voltage V_a must be reduced below the threshold voltage of "T2" of top row, so that it turns "off". Also, the node voltage V_b remains below the threshold voltage of "T2" of bottom row, since "T2" of bottom row and "P2" are designed according to equation 2. When V_a=$V_{t,n}$, the transistor "P1" operates in the linear region while "T1" in saturation. Thus,

$$\frac{\frac{W}{L}_{T1}}{\frac{W}{L}_{P1}} < \frac{2(Vdd - 1.5Vt,n)Vt,n}{(Vdd + 2Vt,p)^2} \quad \text{.....} \quad (3)$$

To summarize, the transistor "T2" of top row will be forced into cut-off mode during the write '0' operation if equation 3 is satisfied. This will ensure that "T2" of bottom row turns on, changing the stored information.

B. Operation of the SRAM cell

We have designed the quaternary SRAM by using following assumption,

The various signals associated with the SRAM cell are:

- 'wr' is the write enable input of the SRAM cell.
- 'in' and 'inb' are the data input nodes.
- Nodes 'a' and 'b' are the data output nodes.

Write Operation:

- During write operation, 'wr' = 1.
- The NMOS pass transistor is in ON state.
- Thus the input is written into the SRAM cell via nodes 'in' and 'inb'.
- Note that inputs at 'in' and 'inb' are complementary to each other.

Read Operation:

- During read operation, 'wr' = 0.
- The NMOS pass transistor is in OFF state.
- Thus the output is read from the SRAM cell via nodes 'a' and 'b'.
- Note that outputs at 'a' and 'b' are complementary to each other.

Table 5 shows the working of quaternary SRAM cell. Simulation results of binary SRAM and quaternary SRAM are shown in figure 10 and figure 11 respectively.

Table V: Working of Quaternary SRAM cell

wr	*SRAM operation*
1	write
0	read

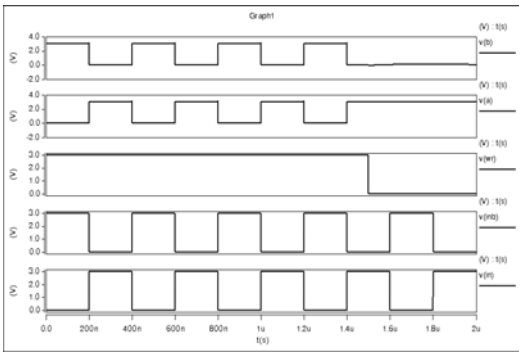

Figure 10: Simulation of Binary SRAM cell

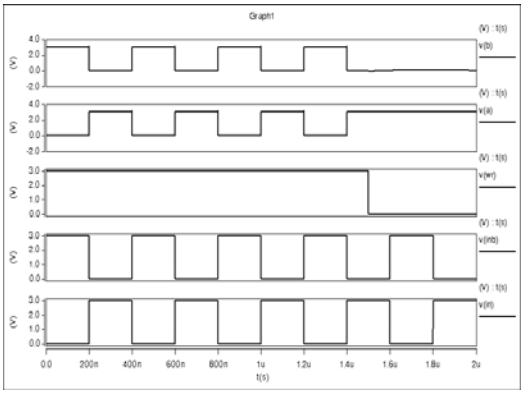

Figure 11: Simulation of Quaternary SRAM cell

C. Design of Binary SRAM cell for comparison purpose.

The binary SRAM circuit is built using two binary inverters as shown in figure 9. Depending on the preserved states of the two-inverter latch circuit, the data being held in the memory cell will be interpreted either as logic '0' or as logic '1'. The control signal 'wr' is used to read data from the memory cell and write data into the memory cell. The 'wr' signal controls the access switches which are essentially NMOS pass transistors. When wr = 1, the pass transistor is on and the data is written into the memory cell. Wr = 0 implies that the write lines are open, and the latest written data will be stored. This is the stabilized data which can be read from nodes 'a' and 'b'.

VI. RESULTS AND COMPARISON

A. Analysis of DRAM

Short channel models [23], with level = 54 is used for 50nm technology node. PTM 90nm technology node with level = 54 is also used for the purpose of comparison. Power analysis of MLDRAM at 90nm and 50nm technology is shown in table 6.The range of dynamic and static power is observed to be same for all logic levels. The circuit behaves well in deep sub micron levels and dynamic power dissipation is reduced approximately to 50% with marginal increase in static power in 50nm technology node when compared to 90nm technology node.

Table VI: Power analysis of MLDRAM at 90 nm and 50 nm technology.

Logic level (cell voltage)	*90 nm technology*		*50 nm technology*	
	Dynamic power	*Static power*	*Dynamic power*	*Static power*
00 (0V)	69.419 µW	2.1127 µW	35.456 µW	2.2528 µW
01 (0.33V)	64.049 µW	1.8916 µW	35.084 µW	2.3710 µW
10 (0.66V)	29.093 µW	1.2494 µW	15.466 µW	1.5506 µW
11 (1V)	40.992 µW	1.2277 µW	17.026 µW	1.3537 µW

B. Analysis of SRAM.

The quaternary and binary SRAM cells were compared and the following results were obtained as shown in table 7 and 8.

Table VII: Quaternary SRAM analysis

Parameters	*Binary SRAM*	*Quaternary SRAM*
Dynamic power dissipation	494n W	446n W
Propagation delay	3.603 ps	7.399 ps
pdp(Ws)	$1.77x10^{-18}$	$3.29x10^{-18}$
no. of transistors	6	14

Table VIII: Static power comparison.

Quaternary	*Binary*		*Qpower nW*	*Bpower nW*
0	0	0	0.465	0.668
1	0	1	1.164	0.668
2	1	0	1.164	0.668
3	1	1	0.465	0.668

VII. CONCLUSION

The success of any DRAM design depends on the efficiency of its sense amplifier. The MLSA presented here can read two bits per cell using quaternary logic. This can be extended to several more bits by using higher level logics. Circuit behaves well at 90nm and 50nm technology nodes

and 50% reduction in dynamic power is observed at 50nm technology node when compared to 90nm. The circuit that has been presented in this paper has the capacity to induce several other developments for the infant field of multi-level logic circuit designing. Advantage of quaternary CMOS SRAM cells include high noise immunity due to larger noise margins obtained by higher power supply voltages, and the ability to operate at lower power supply voltage. The quaternary and binary SRAM cells were compared with the help of Hspice simulation. In quaternary SRAM, less dynamic and static power dissipation is observed, but propagation delay is more than binary SRAM. A quaternary SRAM is equivalent to 2 binary SRAM cells. This is because of the inherent nature of the quaternary logic which can represent 4 different logic levels. Also by using Quaternary SRAM cell, the interconnections, which are the main sources of parasitic capacitance, can be reduced effectively. Thus when quaternary SRAM is employed in a memory array, more power can be saved compared to an array employing binary SRAM cells because of reduced interconnections.

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