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Performance Enhancement Of OTA Using Double Gate MOSFET

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Abstract: Operational Transconductance Amplifier widely used in electronics industry due to its large number of applications.Double gate MOSFETs are strong contenders for nano scale region .In this paper focus will be on designing low input voltage, safer phase margin OTA using double gate MOSFETS. All the simulations are done at 45nm technology.

Keywords: DG MOSFEs, OTA, Analog Tunable circuits, Gain , Phase margin, low supply voltage

I. INTRODUCTION

Electronics devices based on silicon are large such as laptops, palmtops, cellular phones and many more hand held devices. Due to great dealing of silicon based devices, silicon has made system on chip possible. A low voltage and power design to recompensate is required for increasing number of devices on chip. With the breach of 90 nm, silicon industry has moved to nano area to according to ITRS [1]. There are number of problems arises due scaling in conventional bulk CMOS device like SCE's, [2] [3] threshold voltage, non –scaling of vertical dimensions, these problems degrade the performance of circuits and affects the reliability of devices. Double Gate devices have better control over SCE's and junction leakage due to improved electrostatic gate control of back gate [4]. Double Gate MOSFETS are promising devices due to better scalability in nano circuits. With scaling down v_{dd} , v_{gs} also decreases. It allows working in sub threshold region with increased transconductance g_m [5]. Also suitable for analog RF devices because of the capability to handle gigahertz frequency range. By tuning of back gate, provide better characteristics in area , power dissipation and lastly the speed [6] in independent driven mode[IDDG] where two gates are separately biased whereas symmetrically driven mode (SDDG) used in digital applications due to better I_{on}/I_{off} ratio [7]. .In this paper, the basic device structure using DG-MOSFETs is shown, where back gate will be used for the tuned circuit performance. A low power and high gain at 45 nm. OTA using double gate MOSFETs is designed for the study. The simulations are done using spice tool.

II. DG MOSFET STRUCTURE AND FEATURES

The double gates can work in two modes symmetrically driven [SDDG] and independently driven mode [IDDG].The device structure is shown in Fig. 1. The front and back gates are connected to work in symmetrically driven mode and for analog tunable circuits, the front and back gates are biased at different voltages to achieve desired characteristics of device. The gate length is 45 nm. The symmetrical driven mode is better than independently driven mode [IDDG] as discussed in [8] [10-11].

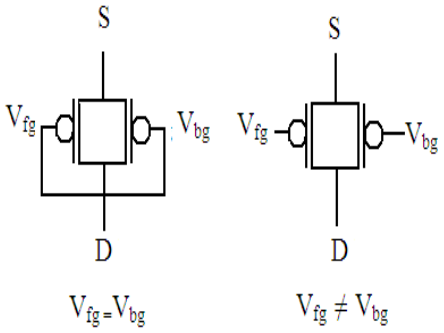

Fig.1 SDDG and IDDG Modes of double-gate MOSFET

III. CONSTRUCTIONAL FEATURES OF DG MOSFET-OTA

Fig.3 shows OTA based double gate MOSFETs. The reported OTA works in independently driven mode and shows very less gain [9].With decreasing gate length, the channel mobility is degraded. Even for shorter channel length, output conductance is increased which will the affect the gain of OTA. In this paper, a new design of OTA to improve gain at 45 nm technology is discussed. The simulations of the existing design have been done using tanner EDA tool version 13.0 at 45 nm CMOS technology for phase response, transient and AC analysis. Existing OTA circuit works at supply voltage of V_{DD} equals to 1.16V and V_{SS} equals to -1.16V respectively. The bandwidth is measured as difference between lower frequency and upper frequency at -3dB down from maximum gain of circuit obtained. As frequency increases, the gain is decreased due to capacitive affects at high frequencies. The open loop gain is function of frequency and shown in equation:

$$A_{OL}(f) = \frac{A}{\sqrt{1+(\frac{f}{fo})^2}} \quad (1)$$

Where A is internal gain and f , f_o are operating frequency and cut-off frequency respectively. The block diagram and circuit symbol is shown in Fig. 2(a) and 2(b) respectively. The open loop gain of existing circuit is observed as 2.6 dB.

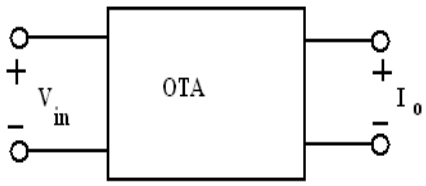

Fig.2 (a) block diagram of OTA

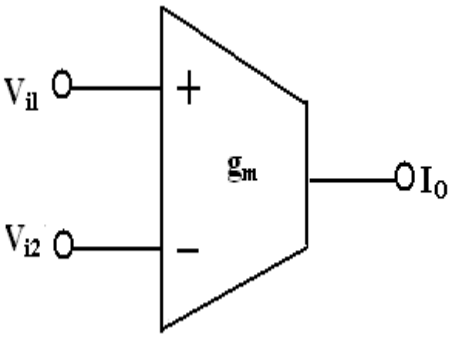

Fig.2 (b) circuit symbol of OTA

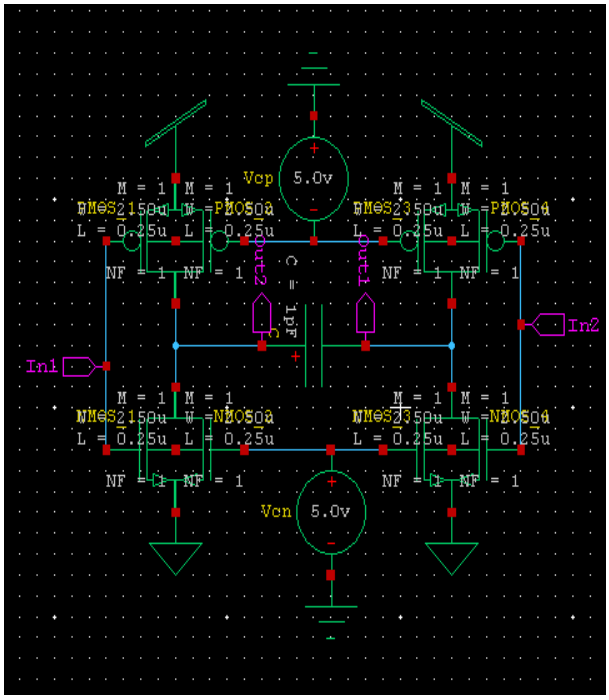

Fig.3 OTA Using Double Gate MOSFET .

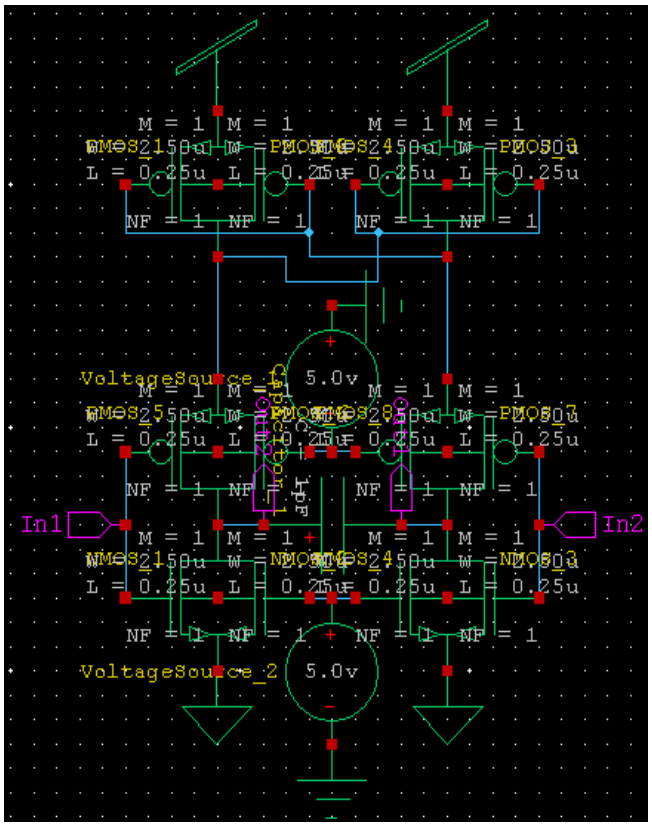

Fig.4 Proposed OTA Circuit.

The proposed OTA works in independently driven mode. The input V_{in1} and V_{in2} are given at back gates through inverters which are also made of double gate MOSFETS. Amplifier transconductance, Gm, is in general a function of the transconductance of transistors at the input stage. It is well known that the transconductance can be increased either by increasing the biasing current of the input transistors or by increasing the size of the input transistors. The proposed OTA works in independently driven mode.. Differential currents flow and charge a load capacitor of 0.1 fF. The loads transistor as active pMOS which gives positive feedback to circuit and increase the gain of circuit. The proposed amplifier will exhibits a positive feedback property. The upper transistor gives positive feedback to circuit which will increase the gain of circuit.

IV. RESULTS

The simulations are done at $V_{dd\ of}$ 0.92 V. and biasing at back gates is v_{cn} = -V_{cp} = 0.1V. The gain is 4.85 dB as shown in Fig.5 (a) .

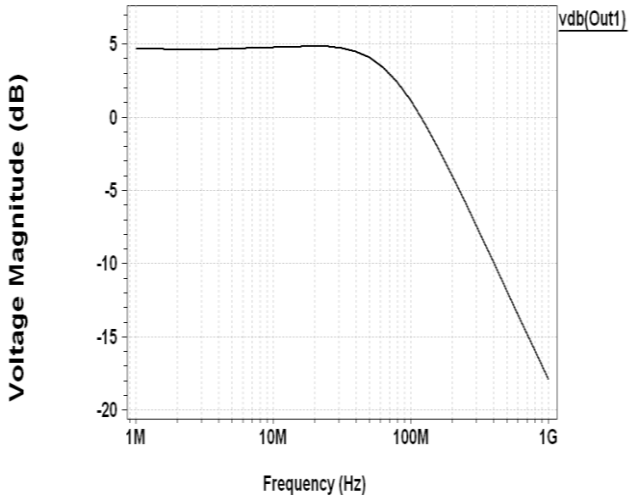

Fig.5 (a) Gain of OTA

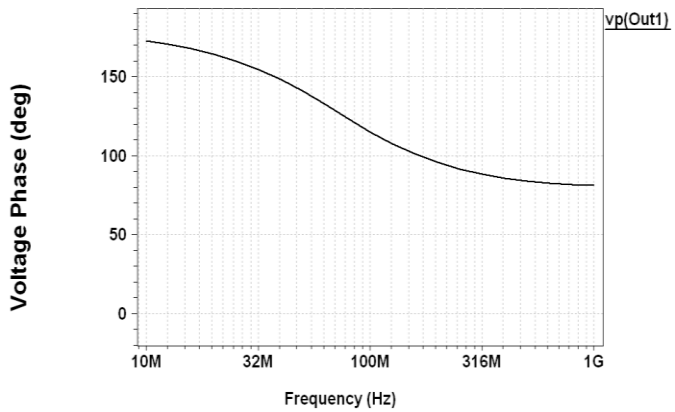

Fig.5 (b) Phase response

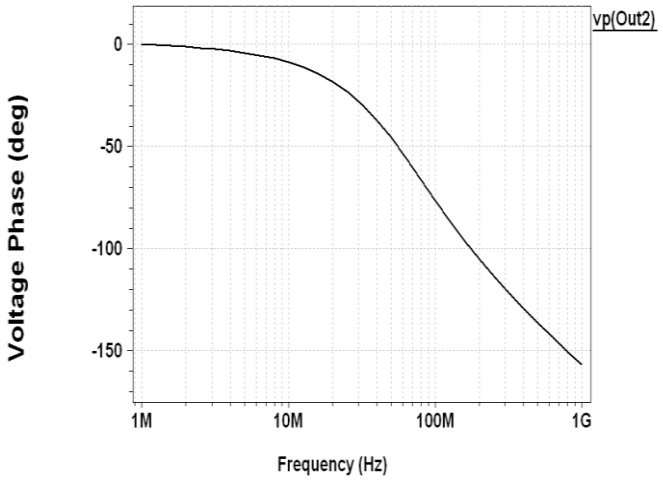

Fig.5(c) Phase Response for input2

TABLE 1

PARAMETERS	Existing OTA	PROPOSED OTA
Phase Margin	60	72
Supply Voltage(V)	1.16	0.92
Gain(dB)	2.6	4.85

V. CONCLUSION

This paper shows appropriateness of double gate MOSFETS for designing of analog circuits like OTA and filters. The designed OTA shows high gain, low power dissipation. The circuit is suitable for high frequency applications and high gain. The proposed circuit is suitable for designing analog filters consists of OTA and capacitor which are also called as integrators. Using double gates, further phase margin, temperature variation and bandwidth will be explored in future.

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