ISSN No. 0976-5697

Volume 3, No. 4, July- August 2012

International Journal of Advanced Research in Computer Science

TECHNICAL NOTE

Available Online at www.ijarcs.info

# An Optimized Multiplier Using Reversible Logic Gates

H.R.Bhagyalakshmi*
Department of Electronics and Communications
BMS College of Engineering
Bangalore,India
hrbbmsce@gmail.com

M.K.Venkatesha
Department of Electronics and Communications,
RNS Institute of Technology
Bangalore, India
mkv2759@yahoo.co.in

***Abstract:*** Reversible logic is very essential for the construction of low power, low loss computational structures which are very essential for the construction of arithmetic circuits used in quantum computation, nano technology and other low power digital circuits. In this paper two designs of an optimized parallel multiplier circuit using reversible logic gates is presented. Multipliers are very essential for the construction of various computational units of a quantum computer. Duplication of operand bits are achieved using two gates namely BVF gate and CFO gate. The multiplier circuit uses DPG gates and a new 4 X 4 reversible logic gate called PPG gate. The proposed work is best compared to the other existing circuits.

***Keywords:*** Reversible logic circuits, Partial products, multiplier, quantum computing, Nanotechnology.

## I. INTRODUCTION

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Quantum computers are constructed using reversible logic circuits. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. In 1960 R. Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware result in energy dissipation due to information loss [1]. According to Landauer's principle, the loss of one bit of information dissipates KTln2 joules of energy where K is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [1]. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. In 1973, Bennett, showed that one can avoid KTln2 joules of energy dissipation constructing circuits using reversible logic gates [2].

## II. REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits [3, 7].

a. The number of Reversible gates (N): The number of reversible gates used in circuit.
b. The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
c. The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
d. Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

Reduction of these parameters is the bulk of the work involved in designing a reversible circuit. In this paper, an improved design of reversible multiplier with respect to its previous counterparts is proposed. Multiplier circuits play an important role in computational operation using computers. There are many arithmetic operations which are performed, on a computer ALU, through the use of multipliers. Design and implementation of digital circuits using reversible logic has attracted popularity to gain entry into the future computing technology.

This paper is organized as follows: Section II gives the brief introduction of the reversible logic gates required for the present work. Section III explains important basic reversible logic gates. Section IV describes the design of multiplier circuit and the implementation of the proposed multiplier circuit using new reversible gates. Section V gives the results and discussions and the comparative study of different designs with the proposed design. Finally Section VI concludes with a scope for further research.

## III. BASIC REVERSIBLE LOGIC GATES

### *A. Feynman gate:*

Fig.1 shows a 2*2 Feynman gate [6]. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1.

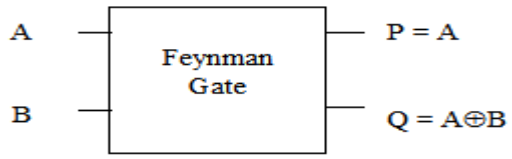


Figure.1. Feynman gate

### *B. Double Feynman Gate (F2G):*

Fig.2 shows a 3*3 Double Feynman gate [7].The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=A⊕B, R=A⊕C. Quantum cost of double Feynman gate is 2.

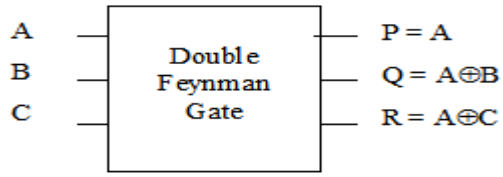


Figure. 2. Double Feynman gate

### *C. Toffoli Gate(TG):*

Fig.3 shows a 3*3 Toffoli gate [3] The input vector is I(A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

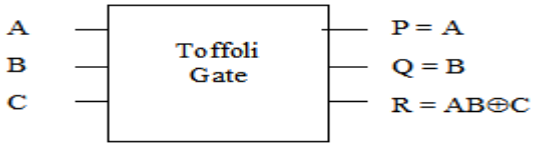


Figure. 3. Toffoli gate

### *D. Peres Gate(TG)*

Fig.4 shows a 3*3 Peres gate [8]. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

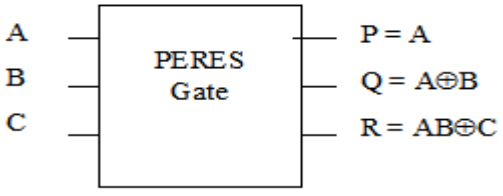


Figure. 4. Peres gate

### *E. Double Peres gate (DPG):*

Fig.5 shows a Double Peres Gate[16]. The full adder using DPG is obtained with C=0 and D= $C_{in}$ and its quantum cost is calculated to be equal to 6 from its quantum realization [11].

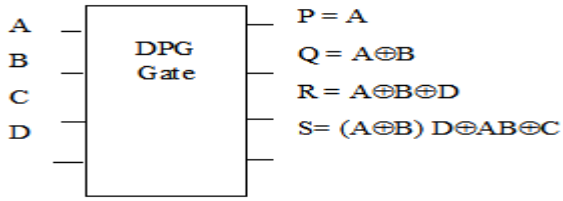


Figure 5. DPG gate

### *F. BVF gate:*

Fig.6 shows a 4 * 4 BVF gate[16]. This is a reversible double XOR gate and can be used for duplication of the required inputs to meet the fan-out requirements. The input vector is I(A,B,C,D) , the output vector is O(P,Q,R,S) and the output is defined by P = A, Q = A⊕B, R = C and S = C⊕D. Quantum cost of a BVF gate is 2.

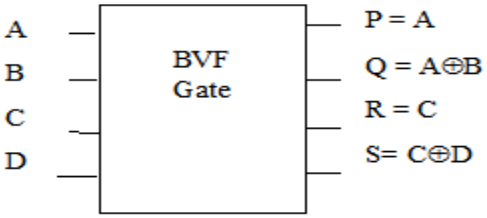


Figure. 6. BVF gate

### *G. CFO gate:*

Fig.7 shows a 4 * 4 CFO gate. The inputs and outputs are as shown in Table-1.This is a reversible triple Feynman gate and can be used for duplication of the inputs to meet the fan-out requirements. The input vector is I(A,B,C,D) , the output vector is O(P,Q,R,S) and the output is defined by P = A, Q = A⊕B, R = A⊕C and S = A⊕D. Quantum cost of a CFO gate is 3.

Table 1: Truth table of CFO gate

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| A | B | C | D | P | Q | R | S |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

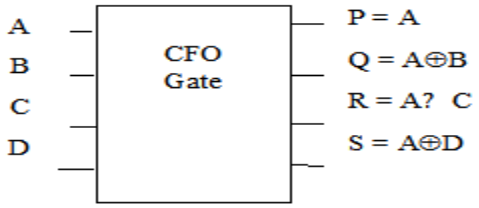


Figure. 7. CFO gate

### *H. Partial Product Generator gate (PPG):*

Fig.8 shows a partial product generator gate (PPG). It is a 4 * 4 gate. It outputs partial products if C input maintained constant at 0. The input vector is I(A,B,C,D) , the output vector is O(P,Q,R,S) and the output is defined by P = A, Q = B, R= AB⊕C and S = AD⊕C. This gate passes two inputs to its outputs and also produces product terms with C input maintained constant at 0 as shown in fig 9. The inputs and outputs are as shown in Table-2. The quantum cost of a PPG gate is 7.

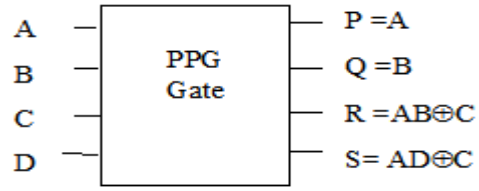


Figure. 8. PPG gate

Table 2: Truth table of PPG gate

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| A | B | C | D | P | Q | R | S |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

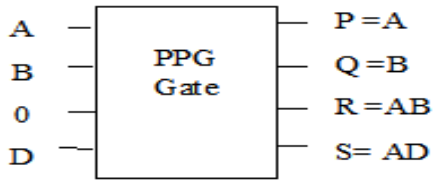


Figure. 9. Product terms with fan-out using PPG gate

## IV. DESIGN OF REVERSIBLE MULTIPLIER

The design of the proposed multiplier uses parallel multiplier is done using two steps.

Part I: Partial Product Generation (PPG)

Part II: Multi-Operand Addition (MOA)

The operation of a 4*4 reversible multiplier is shown in Fig 10. It consists of 16 Partial product bits of the X and Y inputs to perform 4 * 4 multiplications. However, it can extended to any other n * n reversible multiplier.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Partial Product Generation** | | | | | $x_3$ | $x_2$ | $x_1$ | $x_0$ |
| | | | | | $y_3$ | $y_2$ | $y_1$ | $y_0$ |
| | | | | | $P_{03}$ | $P_{02}$ | $P_{01}$ | $P_{00}$ |
| | | | | $P_{13}$ | $P_{12}$ | $P_{11}$ | $P_{10}$ | |
| **Multi operand Addition** | | | $P_{23}$ | $P_{22}$ | $P_{21}$ | $P_{20}$ | | |
| | | $P_{33}$ | $P_{32}$ | $P_{31}$ | $P_{30}$ | | | |
| | $Z_7$ | $Z_6$ | $Z_5$ | $Z_4$ | $Z_3$ | $Z_2$ | $Z_1$ | $Z_0$ |

Figure. 10. The operation of the 4×4 parallel multiplier

### *A. Partial Product Generation(PPG):*

Partial products are generated in parallel using 16 Peres gates [9-12, 14], Fredkin gates in [13, 19] and in [18] modified HNG gates are used for adder part of the multiplier. In [20] authors have presented the design of [16] except the use of BVF gate. In [16] copying of the operands enable fast multiplication as all the product terms are generated with the same delay. In this paper 8 PPG gates are used to generate the same and is a better circuit as it has less hardware complexity and quantum cost compared to other designs [9-20]. The number of constant inputs and number of garbage outputs is reduced by more than 50% which makes this circuit a very optimized compared to the other designs existing in the literature.

In the present design duplication of two input operands of one number is sufficient instead of duplicating all the eight operand bits of two numbers. The number of reversible logic gates of a partial product generator circuit can be reduced by reducing the number of copying gates as well as reducing the number of product generating gates.

There are two ways of duplicating the operands which result in two designs:

***a. Design-1(using CFO gates for copying):*** The fan-out of the inputs y1 and y3 are obtained using the circuit as shown in fig. 12. The circuit uses 2 CFO gates with 6 constant inputs producing zero garbage outputs. The quantum cost of the duplication circuit is 6. The other operands $x_3$, $x_2$, $x_1$, $x_0$ and $y_0$, $y_2$ are used directly.

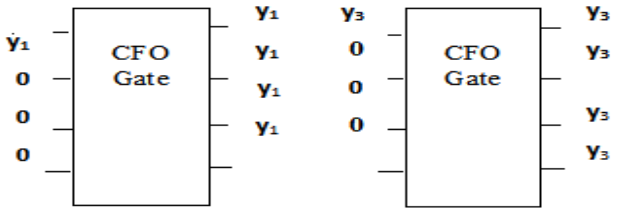


Figure. 11. Fan-out circuit to duplicate the operand bits using CFO gates

***b. Design-2(using BVF gates for copying):*** The fan-out of the inputs y1 and y3 are obtained using the circuit as shown in fig. 11. The circuit uses 3 BVF gates with 6 constant inputs producing zero garbage outputs. The quantum cost of the duplication circuit is 6. The other operands $x_3$, $x_2$, $x_1$, $x_0$ and $y_0$, $y_2$ are used directly.

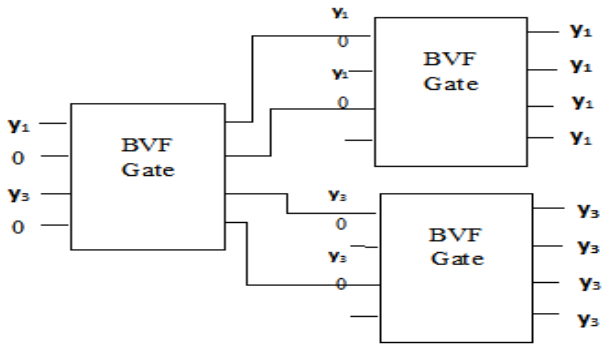


Figure 12. Fan-out circuit to duplicate the operand bits using BVF gates

In [16] authors presented a multiplier circuit where fan-out of operands is achieved using 12 BVF gates .But in this design only two operand inputs instead of four are duplicated using only BVF gates. Remaining 6 operands are used directly and need no duplication. In this design only y1 and y2 are duplicated .

***c. Partial Product Generator circuit:*** The optimized partial product generation is common in both designs. The product terms are generated using 8 PPG gates with 8 constant inputs as shown in fig.13. The product terms are then used as inputs to the multi operand addition circuit. For partial product generation a total of 8 reversible gates with 8 constant inputs are used which produces 4 garbage outputs. The total cost of each PPG block is 62.

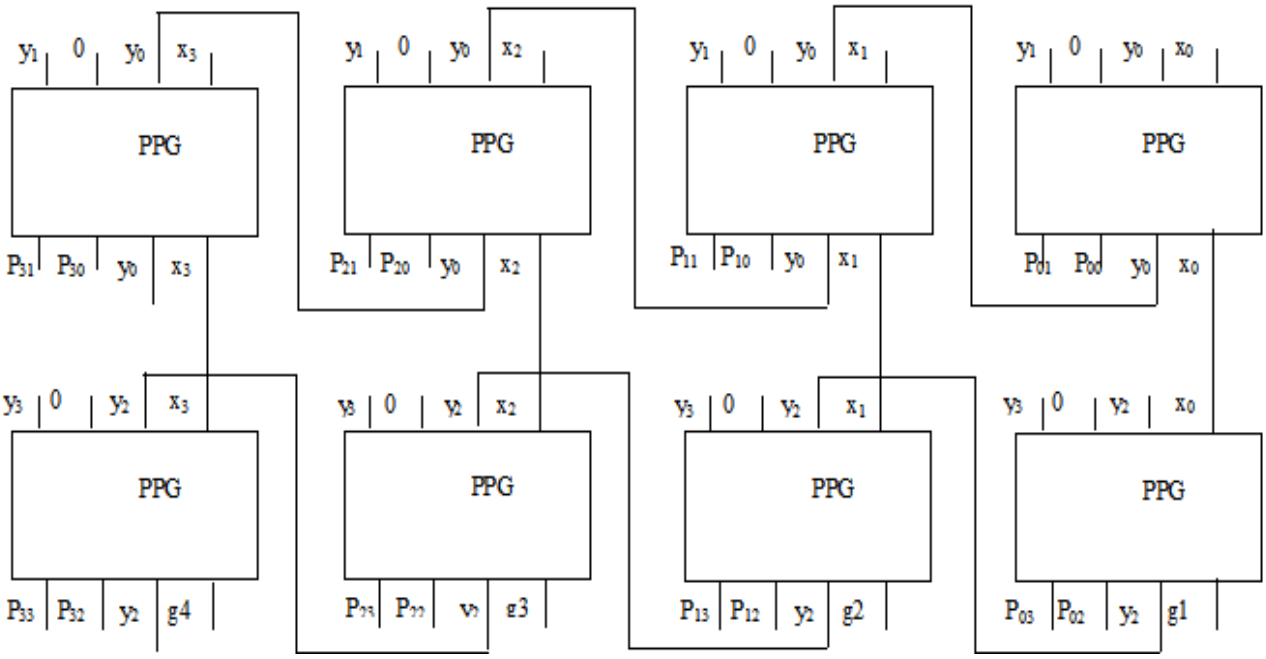


Figure 13. Optimized Partial Product generation circuit using PPG gates

***B. Multi-operand Addition(MOA):***

As proposed in [12], to implement an *n* operand addition circuit part a carry save adder (CSA) is used. The CSA tree reduces the four operands to two. Thereafter, a Carry Propagating Adder (CPA) adds these two operands and produces the final 8-bit product. The proposed four operand adder shown in fig.14 uses DPG gate as a reversible full adder and Peres gate as half adder.

The existing 4*4 gates namely MKG [10], HNG [12], TSG [13], and PFAG [14] can be individually used as an adder. It is shown that use of DPG gate [16] reduces the quantum cost of the multiplier to a minimum value. In the designed reversible multi-operand addition circuit 8 DPG gates and 4 Peres gates are used. The Peres gate half adder has quantum cost of 4 and the DPG adder has quantum cost of 6 and the total quantum cost of multi-operand addition circuit is 64.

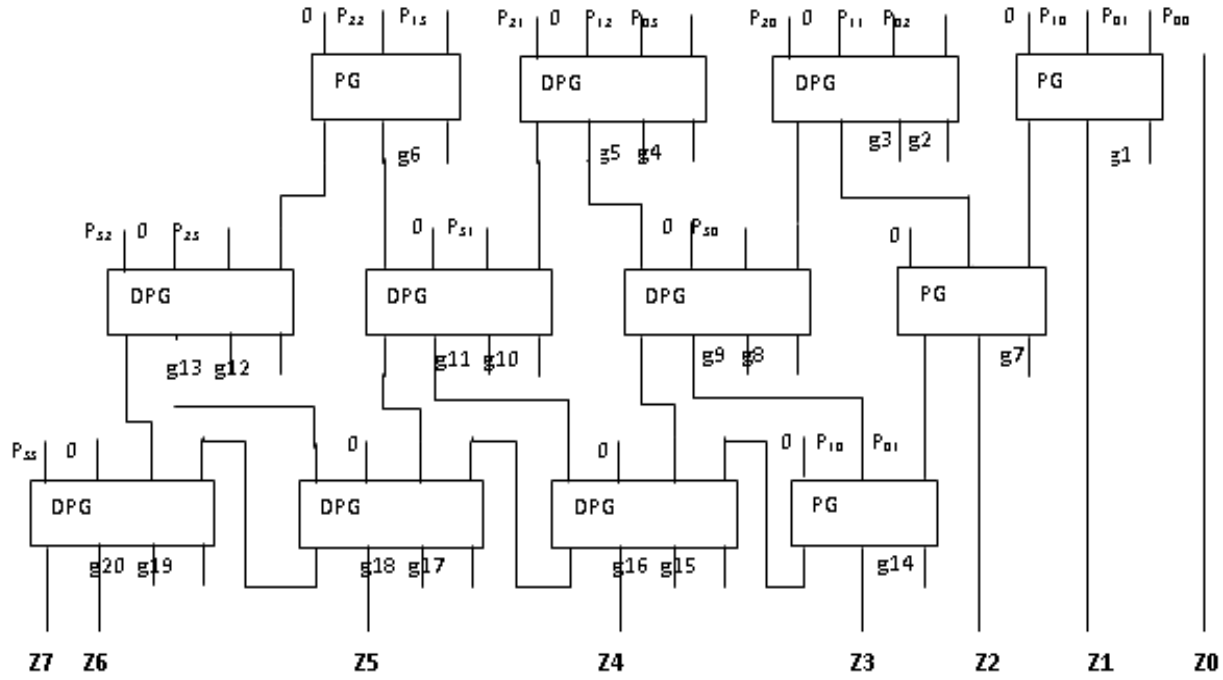


Figure 14. Four-operand Addition (Block diagram)

## V. RESULTS AND DISCUSSION

Hardware complexity is an important factor to decide the total cost of a reversible logic circuit and is expressed in terms ,

A two-input EX-OR calculation = α
A two-input AND calculation = β
A NOT gate calculation = δ

Total logical calculation is = X α + Y β +Z δ (1)

Comparison of different designs of multiplier are as shown in tables 3, 4 and 5. Table-3 gives the comparative study of partial product generation of the circuit and table-4 gives the comparative study of MOA of different designs. Table-5 gives comparison of reversible multipliers.

Table 6 and 7 shows the improvement ratios in terms of various parameters of the presented design-1 and design-2 over the existing designs.

Table 3: Evaluation of different Partial product generators

| Designs | Gate count N | Constant inputs CI | Garbage outputs GO | Quantum cost QC | Logical calculation | Gates used |
|---|---|---|---|---|---|---|
| **Proposed design-1** | **10** | **14** | **8** | **62** | **22α+16β** | **PPG-8; CFO-2** |
| **Proposed design-2** | **11** | **14** | **8** | **62** | **22α+16β** | **PPG-8;BVF-3** |
| Paper[21] | 16 | 16 | 8 | 73 | 23α+16β | PG-7;TG-9 |
| Paper[18] | 16 | 16 | 8 | 73 | 23α+16β | PG-7;TG-9 |
| Paper[20] | 28 | 28 | 20 | 76 | 44α+16β | PG-16;FG-12 |
| Paper[16] | 28 | 40 | 32 | 88 | 46α+16β | PG-16;BVF-12 |
| Paper[9] | 40 | 40 | 32 | 88 | 56α+16β | PG-16, FG-24 |
| Paper[11],[12] | 40 | 40 | 32 | 88 | 56α+16β | PG-16, FG-24 |
| Paper[14] | 40 | 40 | 32 | 88 | 56α+16β | PG-16, FG-24 |
| Paper[10] | 40 | 40 | 32 | 88 | 56α+16β | PG-16, FG-24 |
| Paper[19] | 24 | 32 | 32 | 96 | 46α+64β+32δ | FRG-16;F2G-8 |
| Paper[17] | 28 | 28 | 32 | 104 | 46α+64β+32δ | FRG-16;F2G-8 |
| Paper[13] | 40 | 40 | 32 | 104 | 56α+64β+32δ | FRG-16;FG-24 |

Table-4 gives the comparative study of multi-operand addition of the proposed design with other existing designs assuming minimum quantum cost for HNG, MKG and TSG as 6, 10 and 10 respectively [15].

Table-4: Multi-operand addition (MOA)

| Designs | Gate count N | Constant inputs CI | Garbage outputs GO | Quantum cost QC | Logical calculation | Gates used - |
|---|---|---|---|---|---|---|
| **Proposed design-1** | **12** | **12** | **20** | **64** | **56α+12β** | **PG-4; DPG-8** |
| **Proposed design-2** | **12** | **12** | **20** | **64** | **56α+12β** | **PG-4; DPG-8** |
| Paper[21] | 12 | 12 | 20 | 64 | 48α+16β | PG-4;HNG-8 |
| Paper[18] | 12 | 12 | 14 | 64 | 48α+12β | PG-4;MHNG-8 |
| Paper[20] | 12 | 12 | 20 | 64 | 56α+12β | PG-4; DPG-8 |
| Paper[16] | 12 | 12 | 20 | 64 | 56α+12β | PG-4; DPG-8 |
| Paper[9] | 12 | 12 | 20 | 64 | 56α+12β | PG-4;PFAG-8 |
| Paper[11],[12] | 12 | 12 | 20 | 64 | 48α+16β | PG-4;HNG-8 |
| Paper[14] | 12 | 12 | 20 | 80 | 56α+12β | PG-4;PFAG-8 |
| Paper[10] | 12 | 16 | 24 | 120 | 60α+36β+36δ | MKG-12 |
| Paper[13] | 13 | 18 | 26 | 130 | 78α+39β+39δ | TSG-13 |
| Paper[19] | 20 | 24 | 32 | 140 | 80α+40β+20δ | IG-20 |
| Paper[17] | 20 | 24 | 32 | 140 | 60α+40β+20δ | MIG-20 |

Table-5 gives the comparative study of different reversible multipliers along with their total logical calculation.

Table-5: Reversible multiplier

| Designs | Gate count N | Constant inputs CI | Garbage outputs GO | Quantum cost QC |
|---|---|---|---|---|
| Proposed design-1 | 22 | 26 | 28 | 126 |
| Proposed design-2 | 23 | 26 | 28 | 126 |
| Paper[21] | 28 | 28 | 28 | 137 |
| Paper[18] | 28 | 28 | 22 | 137 |
| Paper[20] | 40 | 40 | 40 | 140 |
| Paper[16] | 40 | 52 | 52 | 152 |
| Paper[9] | 52 | 52 | 52 | 152 |
| Paper[11],[12] | 52 | 52 | 52 | 152 |
| Paper[14] | 52 | 52 | 52 | 168 |
| Paper[10] | 52 | 56 | 56 | 208 |
| Paper[19] | 44 | 56 | 64 | 236 |
| Paper[17] | 48 | 52 | 64 | 244 |
| Paper[13] | 53 | 58 | 58 | 234 |

Table-6 shows the improvement ratio of design-1 in terms of number of gates, number of constant inputs, number of garbage outputs and in terms of quantum cost.

Table-6: Improvement ratios of design-1 with existing designs.

| Designs | Design-1 | | | |
|---|---|---|---|---|
| | Gate count N | Constant inputs CI | Garbage outputs GO | Quantum cost QC |
| Paper[21] | 1.27 | 1.08 | 1.00 | 1.09 |
| Paper[18] | 1.27 | 1.08 | 0.79 | 1.09 |
| Paper[20] | 1.82 | 1.54 | 1.43 | 1.11 |
| Paper[16] | 1.82 | 2.00 | 1.86 | 1.21 |
| Paper[9] | 2.36 | 2.00 | 1.86 | 1.21 |
| Paper[11],[12] | 2.36 | 2.00 | 1.86 | 1.21 |
| Paper[14] | 2.36 | 2.00 | 1.86 | 1.33 |
| Paper[10] | 2.36 | 2.15 | 2.00 | 1.65 |
| Paper[19] | 2.00 | 2.15 | 2.29 | 1.87 |
| Paper[17] | 2.18 | 2.00 | 2.29 | 1.94 |
| Paper[13] | 2.41 | 2.23 | 2.07 | 1.86 |

Table-7 shows the improvement ratio of design-2 in terms of number of gates, number of constant inputs, number of garbage outputs and in terms of quantum cost.

Table-7: Improvement ratios of design-1 with existing designs.

| Designs | Design-2 | | | |
|---|---|---|---|---|
| | Gate count N | Constant inputs CI | Garbage outputs GO | Quantum cost QC |
| Paper[21] | 1.22 | 1.08 | 1.00 | 1.09 |
| Paper[18] | 1.22 | 1.08 | 0.79 | 1.09 |
| Paper[20] | 1.74 | 1.54 | 1.43 | 1.11 |
| Paper[16] | 1.74 | 2.00 | 1.86 | 1.21 |
| Paper[9] | 2.26 | 2.00 | 1.86 | 1.21 |
| Paper[11],[12] | 2.26 | 2.00 | 1.86 | 1.21 |
| Paper[14] | 2.26 | 2.00 | 1.86 | 1.33 |
| Paper[10] | 2.26 | 2.15 | 2.00 | 1.65 |
| Paper[19] | 1.91 | 2.15 | 2.29 | 1.87 |
| Paper[17] | 2.09 | 2.00 | 2.29 | 1.94 |
| Paper[13] | 2.30 | 2.23 | 2.0 | 1.86 |

## VI. CONCLUSIONS

In this paper a new reversible gates called BVF gate and CFO gate is used for the copying of the operand bits of the multiplier. This results in reducing the number of fan-out gates by 50%. This also reduces the total cost and the size of the circuit which are very important design parameters. The proposed multiplier can be used to construct more complex systems in nanotechnology and quantum computers.

## VII. ACKNOWLEDGMENT

The authors wish to thank ECE department of BMS college of Engineering, Bangalore, Karnataka, India for supporting this work

## VIII. REFERENCES


[1]. R. Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp. 183-191, 1961.

[2]. C.H. Bennett, "Logical Reversibility of Computation", IBM J. Research and Development, pp. 525-532, November 1973.

[3]. T. Toffoli., "Reversible Computing", Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science (1980).

[4]. E. Fredkin and T. Toffoli, "Conservative logic," Int'l J. Theoretical Physics, Vol. 21, pp.219–253, 1982.

[5]. Azad Khan, Md. M.H., 2002. Design of full adder with reversible gate. International Conference on Computer and Information Technology, Dhaka, Bangladesh, pp: 515-519

[6]. R. Feynman, "Quantum Mechanical Computers," Optics News, Vol.11, pp. 11–20, 1985.

[7]. B. Parhami; "Fault Tolerant Reversible Circuits" Proc. 40th Asilomar Conf. Signals, Systems, and Computers, Pacific Grove, CA, Oct.2006.

[8]. A. Peres, "Reversible Logic and Quantum Computers", Physical review A, 32:3266- 3276, 1985.

[9]. Fateme Naderpour, Abbas Vafaei "Reversible Multipliers**:** Decreasing the Depth of the Circuit" ICECE 2008, 20-22 December 2008.

[10]. M. Shams, M. Haghparast and K. Navi, "Novel Reversible Multiplier Circuit in Nanotechnology", World Applied Science Journal Vol. 3, No. 5, pp. 806-810, 2008.

[11]. Maryam Ehsanpour , Payman Moallem, Abbas Vafaei, "Design of a Novel Reversible multiplier Circuit Using Modified Full Adder", 2010 International Conference On Computer Design And Applications, 1389, (ICCDA 2010).

[12]. M. Haghparast, S. Jafarali Jassbi, K. Navi and O. Hashemipour, "Design of a Novel Reversible Multiplier Circuit Using HNG Gate in Nanotechnology", World Applied Science Journal Vol. 3 No. 6, pp. 974-978, 2008.

[13]. H. Thapliyal and M.B. Srinivas, "Novel Reversible Multiplier Architecture Using Reversible TSG Gate", Proc. IEEE International Conference on Computer Systems and Applications, pp. 100-103, March 2006.

[14]. M.S. Islam et al., "Low cost quantum realization of reversible multiplier circuit", Information technology journal, 8 (2009) 208.

[15]. Anindita Banerjee and Anirban Pathak 'An analysis of reversible multiplier circuits', arXiv: 0907.3357 (2009), 1-10.

[16]. H. R. Bhagyalakshmi, M. K. Venkatesh, "An Improved Design of a Multiplier using Reversible Logic Gates," in International Journal of Engineering Science and Technology, Vol. 2, No. 8, 2010.

[17]. Somayeh Babazadeh and Majid Haghparast, "Design of a Nanometric Fault Tolerant Reversible Multiplier Circuit",Journal of Basic and Applied Scientific Research, TextRoad Publication, 2(2)1355-1361, 2012,ISSN 2090-4304,www.textroad.com.

[18]. Nidhi Syal, Dr. H.P. Sinha, "High performance reversible parallel multiplier", International Journal of VLSI & Signal processing applications, Vol.1, Issue 3, (21-26), ISSN 2231-3133.

[19]. Nidhi Syal, Dr. H.P. Sinha, "Design of fault tolerant reversible multiplier", International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-1, Issue-6, January 2012.

[20]. Mihail Cutitaru, Lee A. Belfore II, "Improved Cost Reversible Multiplier Design", WORLDCOMP'11 - The 2011 World Congress in Computer Science, Computer Engineering, and Applied Computing, July 18-21,2011,Old Dominion University, Norfolk, Virginia, USA.

[21]. Mohammad Assarian, Majid Haghparast and Keivan Navi, "Delay Reduction in Optimized Reversible Multiplier Circuit",Research Journal of Applied Sciences, Engineering and Technology 4(1): 27-32, 2012