



FAULT TOLERANCE OF ADVANCED IRREGULAR SHUFFLE EXCHANGE NETWORK (AISEN)

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Abstract: Multistage interconnection networks (MINs) are class of high-speed, most efficient interconnection networks (INs) which are used for multiprocessor systems. In present research, fault tolerance is a critical issue. We have proposed a new fault tolerant irregular MIN named as Advanced Irregular Shuffle Exchange Networks (AISEN) and compared it with existing Irregular Augmented Shuffle Exchange Network-2 (IASEN-2) and Modified Alpha Network (MALN). It has better fault tolerance capability as compared to existing IASEN-2 and MALN in terms of non-faulty and faulty conditions.

Keywords: Multistage interconnection networks; fault tolerance; Irregular Augmented Shuffle Exchange Network-2; Modified Alpha Network.

I. INTRODUCTION

Multistage Interconnection Networks (MINs) is a high performance interconnection network, which plays a vital role in parallel processing systems and broadband switching technology. Multistage Interconnection Network (MIN) is formed by many stages of interconnected switches and has low cost and high reliability. Fault tolerance is a critical issue of MIN [7] [9]. A number of regular and irregular networks have been proposed for increasing the ability of fault tolerance in MINs. We propose an Advanced Irregular Shuffle Exchange Network (AISEN) and its routing algorithm, which provide enhanced fault tolerance capacity as compared to MALN and IASEN-2 in terms of different parameters like throughput, processor utilization, processing power, bandwidth etc. AISEN is a single fault tolerant network, it means that network can tolerate fault when a single switch is faulty in every stage. So, AISEN is compared with MALN [3] and IASEN-2 [5] for faulty (single fault) and non-faulty situations.

In this paper, section I presents introduction, section II describes structure of the existing networks, section III describes structure and design of proposed network AISEN. Section IV describes performance evaluation parameter, section V presents Comparison, and Analysis is of proposed network AISEN and existing IASEN-2. At last, conclusion and future work are given in section VI.

II. STRUCTURE OF EXISTING NETWORKS

In MINs, fault tolerance provides alternate path in case of a fault in a link or switch. The proposed network handles switch failure problems and increased performance. Several research works have been done for increasing the fault tolerance of MIN and various networks also have been proposed. This section discuss the basic structure of existing fault tolerant network modified alpha network (MALN) [3] and irregular augmented shuffle exchange networks-2 (IASEN-2)[5].

A. Irregular Augmented Shuffle Exchange Networks-2 (IASEN-2)

IASEN-2 [5], is modified form of IASEN [10] MIN, consists of N number of source address and destination address with $n = \log_2 N$ stages. Each source address is associated with multiplexer (M) of size 2×1 and each destination address associated with demultiplexer (DM) of size 1×2 . Each first and last stage is associated with $N/2$ switching elements (SE). The first stage and last stage have SEs of size 2×3 and 3×2 respectively but SE of second and third stage has size 9×3 and 3×9 respectively. The SEs of each stage is associated with each other through alternative links.

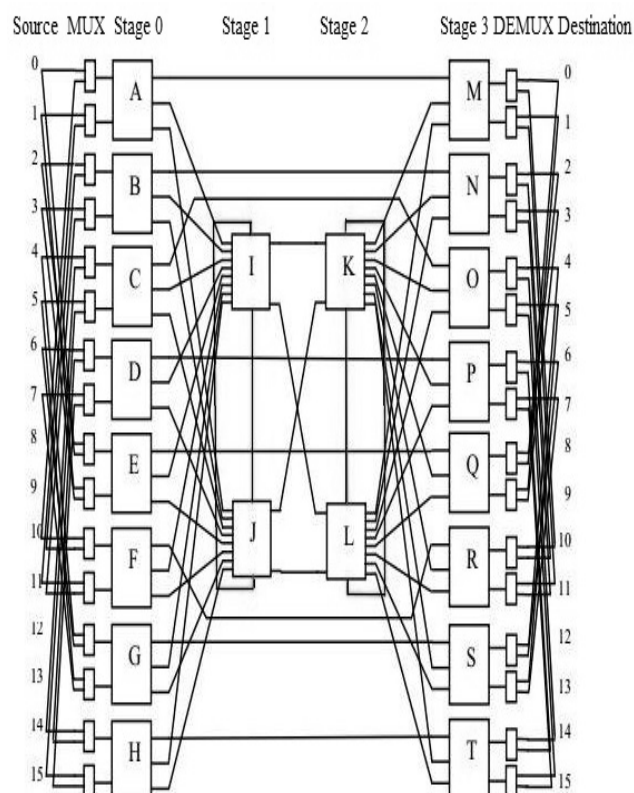


Figure 1. Irregular Augmented Shuffle Exchange Networks-2

B. Modified Alfa Networks (MALN)

Modified Alfa Networks (MALN) [3] consists of $N \times N$ network size with $(2m-2)$ stages where $m = \log_2(N/2)$. All sources and destinations are linked with the multiplexers of size 2×1 and demultiplexers of size 1×2 respectively. All stages except last stage consist of 2^n no. of switching elements (SE) of size 3×3 and the last stage consists of 2^{n-1} no. of switching elements of size 2×2 . The network is divided into two identical sub-networks G_0 and G_1 . If a SE is faulty in any stage then message will be route through auxiliary or alternate link.

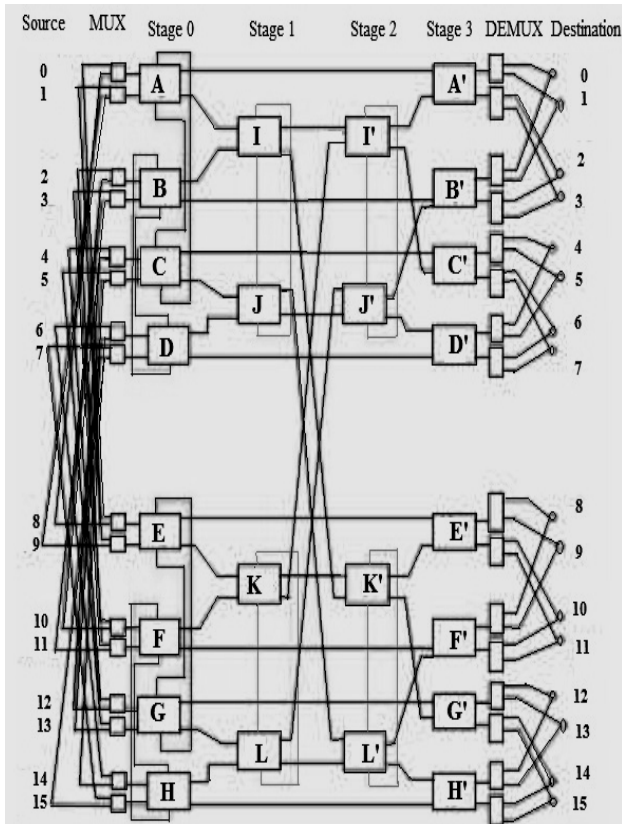


Figure 2. Modified Alfa Networks

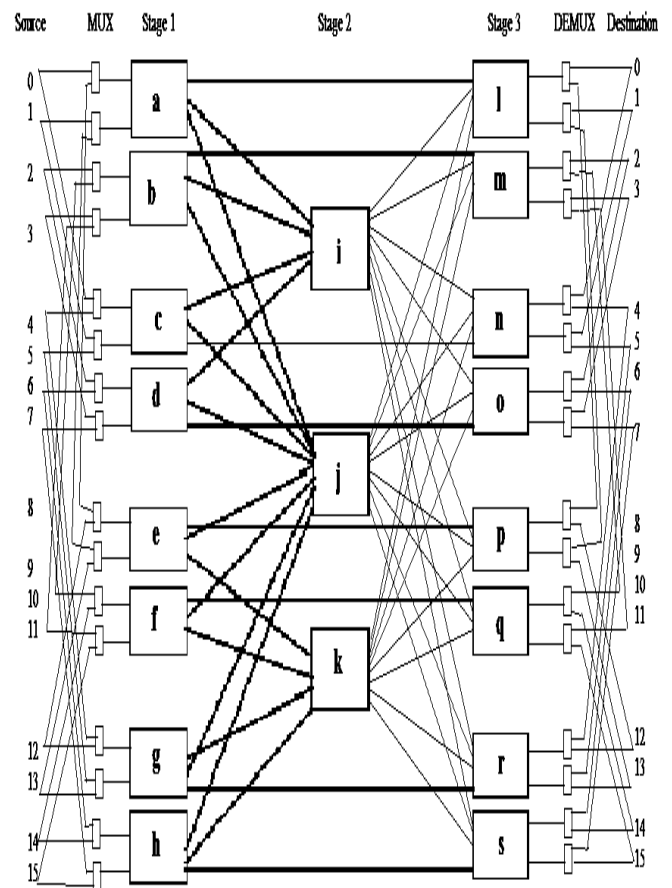


Figure 3. Advanced Irregular Shuffle Exchange Network (AISEN)

In AISEN, SEs of one stage connected with the SEs of next stage as shown in Fig 2. Each source or destination is connected with three SEs of its stage through multiplexer or demultiplexer respectively. For example, source 0 is connected with SE 'a' and SE 'c'. Therefore, we can say that SE 'a' is the Primary SE and SE 'c' first alternate SE. Similarly in second stage, SE 'i', 'j' are primary and first alternate SEs respectively for 'a', 'b', 'c' and 'd' while SE 'j' and 'k' are primary and first alternate for 'e', 'f', 'g', and 'h'. In third stage, SE 'n' and 'l' are primary and first alternate SEs respectively for destination 5. Similarly, we can find primary and first alternate SE for other sources and destinations. Therefore, at least one of the required SE i.e. primary or first alternate SEs of each stage should be in working condition for data transmission from given source to its destinations otherwise network will be failed and data transmission will be stopped.

A. Routing of Proposed Network

In AISEN routing algorithm, the source address, and its corresponding destination address are given. Then data packet is transferred from given source address to its primary switching element (PSE₁) of first stage. If PSE₁ is faulty or busy then data packet will be transferred to its alternate switching element (ASE₁) of first stage. If both of these SEs i.e. PSE₁ and ASE₁ are faulty then it will be considered that network is fail and request will be dropped otherwise send data packet to the primary switching element (PSE₂) of next stage. If primary switching element (PSE₂) of second stage is faulty or busy then data packet will be transferred to alternate switching element (ASE₂) of second stage. If these two i.e. PSE₂ and ASE₂ are faulty then network will be considered as fail and request will be dropped otherwise send data packet to primary switching element (PSE₃) of third stage. If PSE₃ is faulty or

III. PROPOSED INTERCONNECTION NETWORKS

The Advanced Irregular Shuffle Exchange Network (AISEN) is an advanced irregular multistage interconnection networks with $[(\log_2 N) - 1]$ stages, where N is the size of network. First and last stages have $N/2$ switching elements (SE) and second stage has $[(3N)/16]$ SEs. AISEN has N sources and N destinations, which are connected, with N multiplexers (MUX) and N demultiplexers (DEMUX) respectively. In first and last stage, size of each SE is 2×3 and 4×2 respectively. In second stage, there are two types of SEs and their sizes are 4×8 and 8×8 . The second stage consists of $N/8$ number of 4×8 size SEs and $N/16$ number of 8×8 size SEs. Two multiplexer of size 2×1 are connected with each SEs of first stage and two demultiplexer of size 1×2 are connected with each SEs of last stage. Here, a 16×16 network size AISEN is shown in Fig. 2.

busy then send data packet to its alternate switching element (ASE₃) stage third. If both of these SEs i.e. PSE₃ and ASE₃ are faulty then network will be considered as fail and request will be dropped otherwise data packet will be transferred to its given destination address.

S_t= total number of stages
 T= If network is non-faulty, then data transmission time
 T_{SF}= If network is single switch faulty, then data transmission time.

IV. PERFORMANCE EVALUATION PARAMETERS

Between each source-destination pair, the data packet takes the minimum path in data transmission process when the network is non-faulty (or no fault in switches). The data packet is rerouted from faulty node to non-faulty node if a single switch fault occurs in network. Thus, the routing time of data packets between two nodes will be double in faulty case as compared to non-faulty case. For example, let the routing time of data packets between two non-faulty nodes is 0.01 ms and for single switch fault is 0.02 ms [6].

C. Bandwidth

“The average number of dynamic memory modules per unit time is known as bandwidth” [1][2][3]. For S_n sources and D_n destinations, the bandwidth is calculated as follows:

$$BW = D_n \times p_n$$

D. Probability of Acceptance (PA)

“PA is the number of request acknowledged by the destination side, which is sent by the source side in a transmission cycle”[1][2][4]. It is calculated as follows:

$$PA = [BW / (D_n \times p)]$$

E. Throughput

“The average number of data or information packets transferred successfully from a source to destination pair in a MIN is known as throughput” [1][2][4]. In other words, the maximum number of traffic acknowledged by a MIN per unit time is called throughput.

$$TP = BW / (D_n \times T)$$

F. Processor Utilization (PU)

“PU is the percentage of time the processor is dynamic doing calculation without getting to the global memory” [1][2][4].

$$PU = BW / (D_n \times p \times T)$$

G. Processing Power (PP)

Processing power can be determined on behalf of processor. The aggregate of processor utilization over the number of processors is called processing power. It is given as follows:

$$PP = (N \times PU)$$

V. COMPARISON AND ANALYSIS

In this section, the performance analysis is calculated with the help of performance evaluation parameters for IASEN-2 [5], MALN [3] and AISEN and their comparison is also performed in faulty (or single switch fault) non-faulty conditions. Let the data packets are transferred from source 1 to destination 4. We assume that the routing time between two nodes is 0.01 ms in non-faulty condition and 0.02 ms for faulty (or single switch fault) condition. The node can be anything such as source, destination, or SE. Let the value of request generation probability or offered load (p) is 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, and 1. The results of comparison and analysis among MALN, IASEN-2, and AISEN are shown below:

A. Bandwidth (BW)

Bandwidth of AISEN is better than IASEN-2 and MALN in both conditions.

A. Request Generation Probability (p)

The number of data or information packets delivered on a source node and these packets can be conveyed to N destinations over MINs is known as Request Generation Probability (p) or Load Factor [1][2]. The value of p is assumed to be 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, and 1.

Let ‘a’ and ‘b’ are inputs and outputs of a switching element (SE) respectively and the request generation probability for each a×b switch is p. Thus, general probability equation is as follows:

Probability [1],[2],[4] that one output receiving the request from ‘a’ inputs is:

$$P_n = [1 - (1 - (p/b))^a] \tag{1}$$

Probability equation for IASEN-2:

$$p_1 = 1 - (1 - p/2)^2 \tag{2}$$

$$p_2 = 1 - (1 - p_1/6)^9 \tag{3}$$

$$p_3 = 1 - (1 - p_2/9)^3 \tag{4}$$

$$p_4 = 1 - [(1 - p_3) \times (1 - p_1/2)]^2 \tag{5}$$

Probability equation for MALN:

$$p_1 = 1 - (1 - p_0/3)^3 \tag{6}$$

$$p_2 = 1 - (1 - p_1/6)^3 \tag{7}$$

$$p_3 = 1 - (1 - p_2/3)^3 \tag{8}$$

$$p_4 = 1 - \{(1 - p_3) \times (1 - p_1/2)\}^2 \tag{9}$$

Probability equation for AISEN:

Request generation probability for first stage

$$p_1 = 1 - (1 - p/3)^2 \tag{10}$$

Request generation probability for second stage

$$p_{20} = 1 - (1 - P_1/8)^4 \tag{11}$$

$$p_{21} = 1 - (1 - P_1/8)^8 \tag{12}$$

$$p_{22} = 1 - (1 - P_1/8)^4 \tag{13}$$

$$p_2 = (P_{20} + P_{21} + P_{22})/3 \tag{14}$$

Request generation probability for third stage

$$p_3 = 1 - [(1 - P_2) \times (1 - P_1/2)]^4 \tag{15}$$

B. Data Transmission Time

It is time that all generated data packets take from source to the given number of destinations [8].

If network is non-faulty, then it is given as follows:

$$T = (N_n - 1) \times T_n \times N_{dp} \times D_n$$

If network has single switch fault, then it is given as follows:

$$T_{SF} = T_D + (S_t \times T)$$

Where, N_n=Number of nodes including source and destination

T_n= Routing Time between two nodes

D_n=Number of destinations

N_{dp}= Total number of generated data packets on a source node

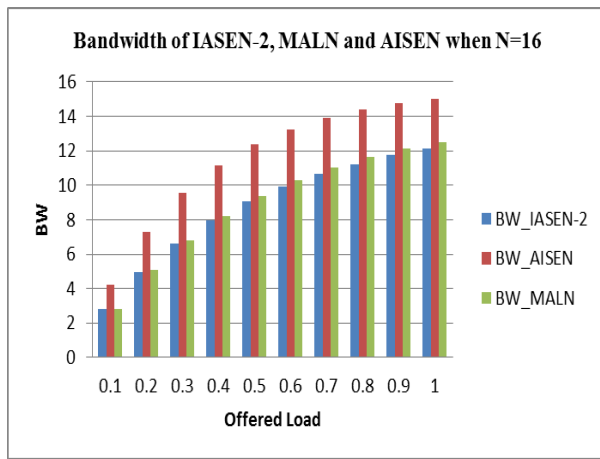


Figure 4. Bandwidth Comparison of IASEN-2, MALN, and AISEN

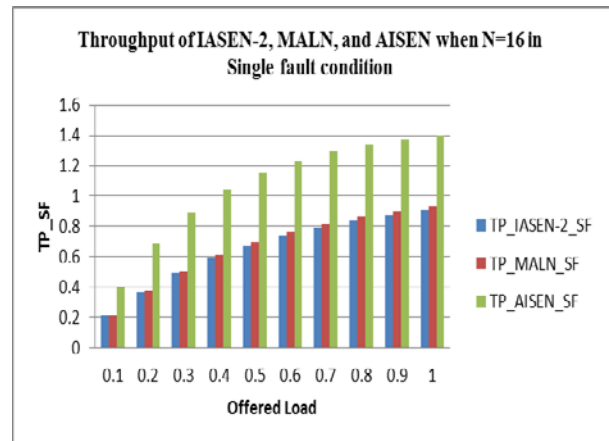


Figure 7. Throughput Comparison of IASEN-2, MALN, and AISEN under Single switch fault condition

B. Probability of Acceptance (PA)

Probability of Acceptance of AISEN is greater than IASEN-2 and MALN.

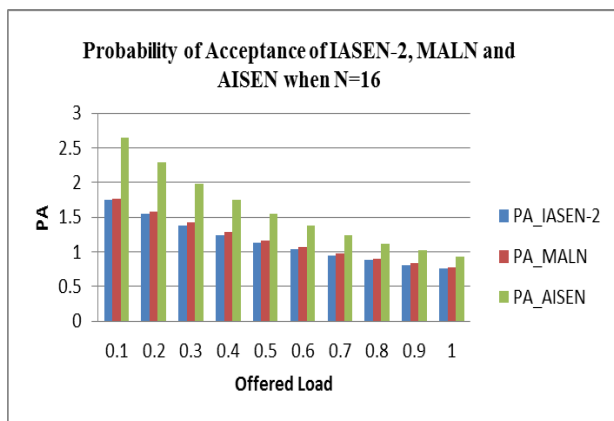


Figure 5. Probability of Acceptance Comparison of IASEN-2, MALN, and AISEN

C. Throughput (TP)

Performance comparison of throughput is given in Fig. 6 and Fig. 7. in non-faulty (without fault) and faulty (single switch fault) conditions respectively.

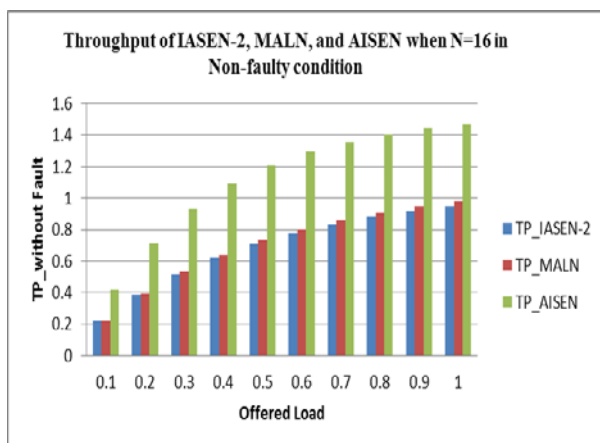


Figure 6. Throughput Comparison of IASEN-2, MALN, and AISEN under non-faulty condition

Therefore, throughput of AISEN is greater than throughput of IASEN-2 and MALN under faulty (single switch fault) and non-faulty environment.

D. Processor Utilization (PU)

Processor utilization of AISEN is better than IASEN-2 and MALN in both conditions.

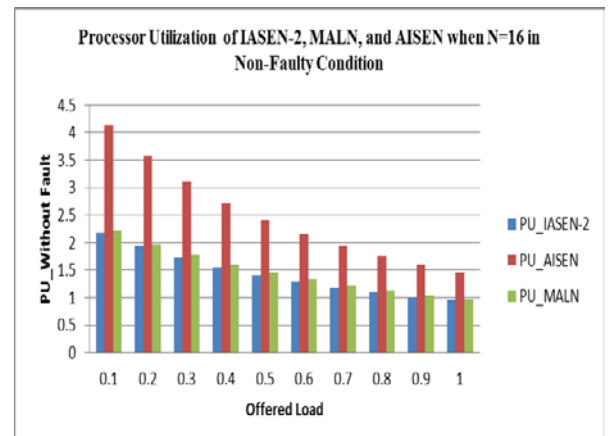


Figure 8. Processor Utilization Comparison of IASEN-2, MALN, and AISEN under non-faulty condition

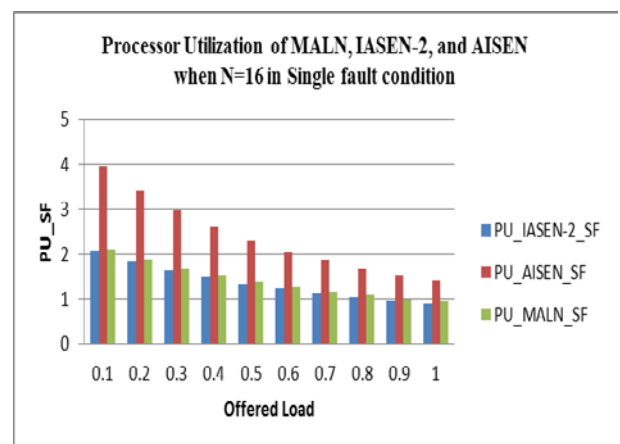


Figure 9. Processor Utilization Comparison of IASEN-2, MALN, and AISEN under Single switch fault condition

E. Processing Power (PP)

Processing Power (PP) of AISEN is greater than PP of IASEN-2 and MALN under faulty and non-faulty environment.

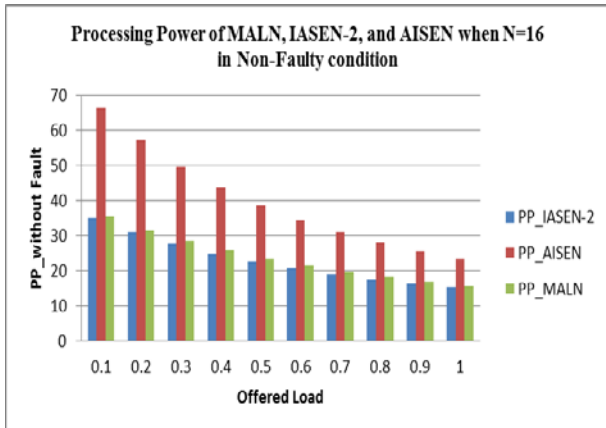


Figure 10. Processing Power Comparison of IASEN-2, MALN, and AISEN under non-faulty condition

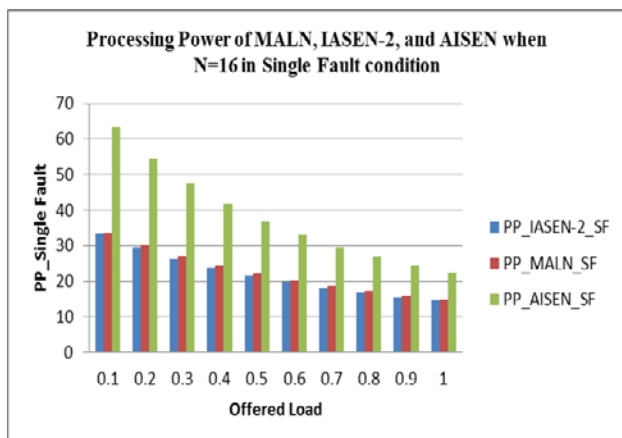


Figure 11. Processing Power Comparison of IASEN-2, MALN, and AISEN under Single switch fault condition

VI. CONCLUSION

In this paper, the proposed fault tolerant MIN performs better than the IASEN-2 and MALN. The routing algorithm and

performance analysis shows that AISEN is a single switch fault tolerant MIN at each stage of the network and performs data transmission efficiently. The network design of AISEN can be changed and applied on other MINs to obtain more fault tolerant network at optimum cost in future.

VII. REFERENCES

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